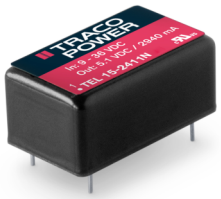
TEL 15N Datasheet 2
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TRACO POWER

DC/DC Converter

TEL 15N Series, 15 Watt

- **Ultra compact 15 Watt converter in DIP-16 metal casing**
- **Highest power density of 4.51 W/cm3**
- **Operating temperature range -40°C to +85°C**
- **Wide 2:1 input voltage ranges: 9-18, 18-36, 36-75 VDC**
- **High efficiency (up to 87%) for low thermal loss**
- **6-side shielded metal case with insulated baseplate**
- **Built-In EN 55032 class A filter (conducted)**
- **Protection against short circuit**
- **3-year product warranty**



UL 62368-1 IEC 62368-1

The TEL 15N is a series of isolated 15 Watt converters which come in an ultra compact DIP-16 metal package. The design purpose of this series was to miniaturized low power DC/DC converters to the maximum without sacrificing high efficiency. It solidifies the new standard for power density with 4.51 W/cm3 and effectively doubles the power density compared to 15 Watt converters in DIP-24 packages. The TEL 15N offers a wide 2:1 input voltage range and features a high efficiency of up to 87% which enables an operation temperature of up to +55°C at full load and up to 85°C with 50% load. The converters also have an internal input filter to comply with conducted emission standard EN 55032 class A. It's an economical solution for space critical and cost sensitive applications in instrumentation, IT and industrial electronics.

Models

Order Code	Input Voltage Range	Output 1		Output 2		Efficiency
		Vnom	Imax	Vnom	Imax	typ.
TEL 15-1211N	9 - 18 VDC (12 VDC nom.)	5.1 VDC	2'940 mA			86 %
TEL 15-1212N		12 VDC	1'250 mA			87 %
TEL 15-1213N		15 VDC	1'000 mA			87 %
TEL 15-1215N		24 VDC	625 mA			87 %
TEL 15-1222N		+12 VDC	625 mA	−12 VDC	625 mA	87 %
TEL 15-1223N		+15 VDC	500 mA	−15 VDC	500 mA	87 %
TEL 15-2411N	18 - 36 VDC (24 VDC nom.)	5.1 VDC	2'940 mA			86 %
TEL 15-2412N		12 VDC	1'250 mA			87 %
TEL 15-2413N		15 VDC	1'000 mA			87 %
TEL 15-2415N		24 VDC	625 mA			87 %
TEL 15-2422N		+12 VDC	625 mA	−12 VDC	625 mA	87 %
TEL 15-2423N		+15 VDC	500 mA	−15 VDC	500 mA	87 %
TEL 15-4811N	36 - 75 VDC (48 VDC nom.)	5.1 VDC	2'940 mA			86 %
TEL 15-4812N		12 VDC	1'250 mA			87 %
TEL 15-4813N		15 VDC	1'000 mA			87 %
TEL 15-4815N		24 VDC	625 mA			87 %
TEL 15-4822N		+12 VDC	625 mA	−12 VDC	625 mA	87 %
TEL 15-4823N		+15 VDC	500 mA	−15 VDC	500 mA	87 %

Note - 48 Vin models: If the input will be switched electromechanically, use an external 27 µF / 200 V / KXY capacitor to reduce voltage transient.

Input Specifications

Input Current	- At no load	12 Vin models:	20 mA typ.
		24 Vin models:	10 mA typ.
		48 Vin models:	7 mA typ.
	- At full load	12 Vin models:	1'450 mA typ.
		24 Vin models:	720 mA typ.
		48 Vin models:	360 mA typ.
Surge Voltage		12 Vin models:	25 VDC max. (1 s max.)
		24 Vin models:	50 VDC max. (1 s max.)
		48 Vin models:	100 VDC max. (1 s max.)
Under Voltage Lockout		12 Vin models:	8 VDC typ.
		24 Vin models:	16 VDC typ.
		48 Vin models:	34 VDC typ.
Recommended Input Fuse		12 Vin models:	3'000 mA (slow blow)
		24 Vin models:	1'500 mA (slow blow)
		48 Vin models:	1'000 mA (slow blow)
			(The need of an external fuse has to be assessed in the final application.)
Input Filter			Internal Pi-Type

Output Specifications

Voltage Set Accuracy			±1% max.
Regulation	- Input Variation (Vmin - Vmax)	single output models:	0.8% max.
		dual output models:	0.8% max.
	- Load Variation (0 - 100%)	single output models:	1% max.
		dual output models:	1% max. (Output 1)
			1% max. (Output 2)
	- Voltage Balance (symmetrical load)	dual output models:	2% max.
	- Cross Regulation (25% / 100% asym. load)	dual output models:	5% max.
Ripple and Noise	- 20 MHz Bandwidth		70 mVp-p typ. (w/ 2.2 µF / 50 V MLCC)
Capacitive Load	- single output	5.1 Vout models:	1'800 µF max.
		12 Vout models:	820 µF max.
		15 Vout models:	820 µF max.
		24 Vout models:	270 µF max.
	- dual output	12 / -12 Vout models:	560 / 560 µF max.
		15 / -15 Vout models:	270 / 270 µF max.
Minimum Load			Not required
Temperature Coefficient			±0.02 %/K max.
Start-up Time			40 ms max.
Short Circuit Protection			Continuous, Automatic recovery (Hiccup Mode, Automatic Recovery)
Output Current Limitation			110% min. of Iout max.
			160% typ. of Iout max.
Transient Response	- Response Deviation		3% typ. / 5% max. (75% to 100% Load Step)
	- Response Time		500 µs max. (75% to 100% Load Step)

Safety Specifications

Standards	- IT / Multimedia Equipment	EN 62368-1
		IEC 62368-1
		UL 62368-1
	- Certification Documents	www.tracopower.com/tel15n-safety-cert/
Energy Source	- Output, acc. to 62368-1	ES1
Power Source	- Output, acc. to 62368-1	PS2

All specifications valid at nominal voltage, resistive full load and +25°C after warm-up time, unless otherwise stated.

Pollution Degree			PD 3
Over Voltage Category			Not mains connected

EMC Specifications

EMI (Emissions)	- Conducted Emissions		EN 55032 class A (internal filter)
			EN 55032 class B (with external filter)
	- Radiated Emissions		EN 55032 class A (with external filter)
			EN 55032 class B (with external filter)
		External filter proposal:	www.tracopower.com/tel15n-emc-filter/
EMS (Immunity)			EN 55024 (IT Equipment)
			EN 55035 (Multimedia)
	- Electrostatic Discharge	Air:	EN 61000-4-2, ±8 kV, perf. criteria A
		Contact:	EN 61000-4-2, ±6 kV, perf. criteria A
	- RF Electromagnetic Field		EN 61000-4-3, 20 V/m, perf. criteria A
	- EFT (Burst) / Surge		EN 61000-4-4, ±2 kV, perf. criteria A
			EN 61000-4-5, ±2 kV, perf. criteria A
		External filter proposal:	www.tracopower.com/tel15n-emc-filter/
	- Conducted RF Disturbances		EN 61000-4-6, 10 Vrms, perf. criteria A
	- PF Magnetic Field	Continuous:	EN 61000-4-8, 30 A/m, perf. criteria A
EMC / Environmental	- Certification Documents		www.tracopower.com/tel15n-emc-cert/

General Specifications

Relative Humidity			95% max. (non condensing)
Temperature Ranges	- Operating Temperature		–40°C to +80°C
	- Case Temperature		+110°C max.
	- Storage Temperature		–50°C to +125°C
Power Derating	- High Temperature		1.9 %/K above 55°C (average)
		See application note:	www.tracopower.com/tel15n-cc/
Cooling System			Natural convection (20 LFM)
Altitude During Operation			6'000 m max.
Regulator Topology			Flyback Converter
Switching Frequency			420 - 540 kHz (PWM)
Insulation System			Functional Insulation
Isolation Test Voltage	- Input to Output, 60 s		1'500 VDC
	- Input to Output, 1 s		1'800 VDC
	- Input to Case, 60 s		1'000 VDC
	- Output to Case, 60 s		1'000 VDC
Isolation Resistance	- Input to Output, 500 VDC		1'000 MΩ min.
Isolation Capacitance	- Input to Output, 100 kHz, 1 V		2'200 pF max.
Reliability	- Calculated MTBF		2'150'000 h (MIL-HDBK-217F, ground benign)
Washing Process			According to Cleaning Guideline www.tracopower.com/info/cleaning.pdf
Environment	- Vibration		2.4 g, 3 axis, random waveform, 30 min
	- Mechanical Shock		30 g, 3 axis, half sine, 11 ms
	- Thermal Shock		IPC-9592B
Housing Material			Aluminum
Potting Material			Silicone (UL 94 V-0 rated)
Pin Material			Copper Alloy (C6801)
Pin Foundation Plating			Nickel (2 - 4 µm)
Pin Surface Plating			Tin (3 - 5 µm), matte
Housing Type			Metal Case
Mounting Type			PCB Mount
Connection Type			THD (Through-Hole Device)
Footprint Type			DIP16
Soldering Profile			Lead-Free Wave Soldering 260°C / 10 s max.

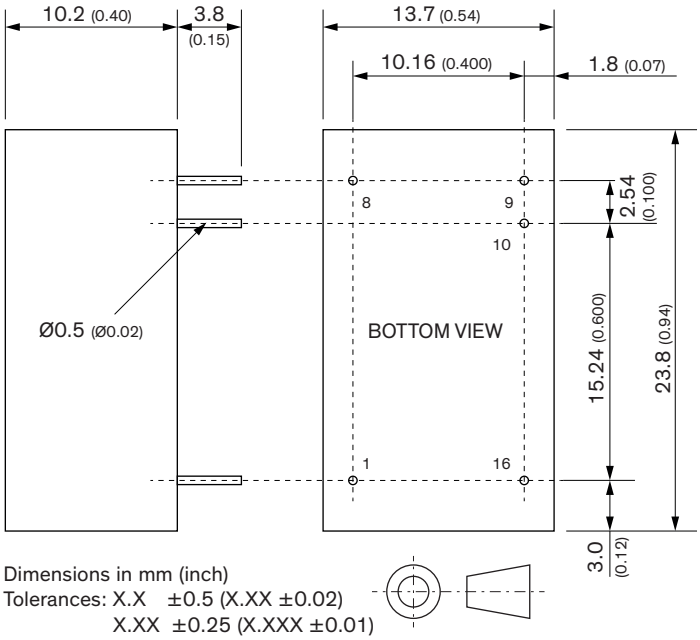
All specifications valid at nominal voltage, resistive full load and +25°C after warm-up time, unless otherwise stated.

Weight		8.8 g
Thermal Impedance	- Case to Ambient	24.6 K/W typ.
Environmental Compliance	- REACH Declaration	www.tracopower.com/info/reach-declaration.pdf
		REACH SVHC list compliant
		REACH Annex XVII compliant
	- RoHS Declaration	www.tracopower.com/info/rohs-declaration.pdf
		Exemptions: 7(a)
		(RoHS exemptions refer to the component concentration only, not to the overall concentration in the product (O5A rule).)
	- SCIP Reference Number	e74ab8fa-1d15-4362-954c-972163d70177

Additional Information

Supporting Documents	www.tracopower.com/overview/tel15n
Frequently Asked Questions	www.tracopower.com/glossary-faq
Glossary	www.tracopower.com/info/glossary.pdf
Service Portal	www.tracoserviceportal.com

Outline Dimensions



Dimensions in mm (inch)
Tolerances: X.X ±0.5 (X.XX ±0.02)
X.XX ±0.25 (X.XXX ±0.01)
Pin diameter tolerances: X.X ±0.05 (X.XX ±0.002)

Pinout		
Pin	**Single**	**Dual**
1	–Vin	
8	NC	Common
9	+Vout	
10	–Vout	
16	+Vin	

NC: Not connected

Avoid routing PCB traces under the converter.

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TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C and HDMI 2.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±12-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2 A (8/20 µs)
- IO Capacitance:
  - 0.25 pF (Typical)
  - 0.33 pF (Maximum)
- DC Breakdown Voltage: 5.5 V (Minimum)
- Ultra Low Leakage Current: 10 nA (Maximum)
- Low ESD Clamping Voltage: 8.8 V at 5-A TLP
- Supports High Speed Interfaces up to 10 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Easy Flow-Through Routing Package

2 Applications

- End Equipment
  - Laptops and Desktops
  - Set-Top Boxes
  - TV and Monitors
  - Mobile and Tablets
  - DVR and NVR
- Interfaces
  - USB Type-C
  - USB 3.1 Gen 2
  - HDMI 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3.0

3 Description

The TPD4E02B04 is a bidirectional TVS ESD protection diode array for USB Type-C and HDMI 2.0 circuit protection. The TPD4E02B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.25-pF IO capacitance per channel making it ideal for protecting high-speed interfaces up to 10 Gbps such as USB 3.1 Gen2. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

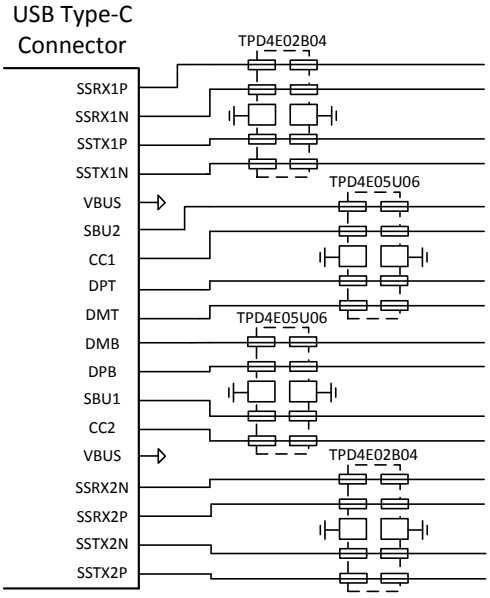
The TPD4E02B04 is offered in the industry standard USON-10 (DQA) package. The package features flow-through routing and 0.5-mm pin pitch easing implementation and reducing design time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E02B04	USON (10)	2.50 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2016) to Revision B **Page**

- Updated Capacitance spec in the *Features*, *Description*, , *IO Capacitance* and *Operating Frequency* sections ... 1
- Made changes to *Operating Frequency* ... 1
- Updated Figure 15, Figure 16, Figure 22 and Figure 23 ... 1

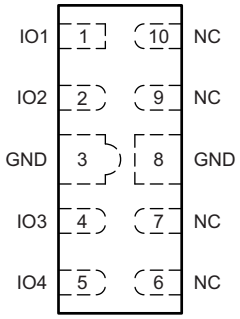
Changes from Original (Novemeber 2015) to Revision A **Page**

- Changed device status from *Product Preview* to *Production Data* ... 1

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5 Pin Configuration and Functions

DQA Package
10-Pin USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs)		17	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		2	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD4E02B04 DQA (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	214.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	270.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	81.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	270.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, any IO pin to GND(1)	I_{IO} = 1 mA, T_A = 25°C	5.5	6.4	7.5	V
V_{BRR}	Breakdown voltage, GND to any IO pin(1)	I_{IO} = 1 mA, T_A = 25°C	–5.5	–6.4	–7.5	V
V_{HOLD}	Holding voltage(2)	I_{IO} = 1 mA		5.8		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		6.6		V
		I_{PP} = 5 A, TLP, from IO to GND		8.8		
		I_{PP} = 1 A, TLP, from GND to IO		6.6		
		I_{PP} = 5A, TLP, from GND to IO		8.8		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.47		Ω
		GND to IO		0.47		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.25	0.33	pF
ΔC_L	Variation of line capacitance	Delta of capacitance between any two IO pins, V_{IO} = 0 V, f = 1 MHz, T_A = 25°C, GND = 0 V		0.01	0.07	pF
C_{CROSS}	Channel to channel capacitance	Capacitance from one IO to another, V_{IO} = 0 V, f = 1 MHz, GND = 0 V		0.13		pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied in the negative-going direction, after the device has successfully latched into the snapback state.

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6.7 Typical Characteristics

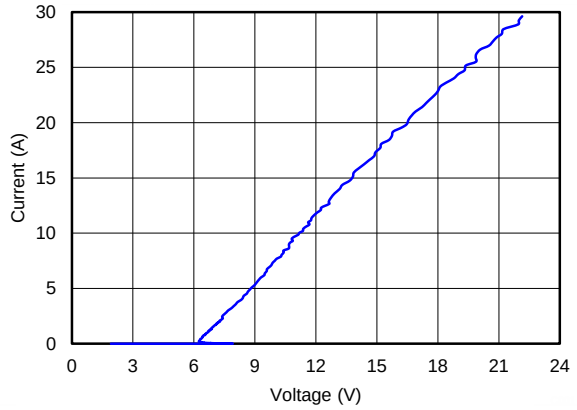


Figure 1. Positive TLP Curve

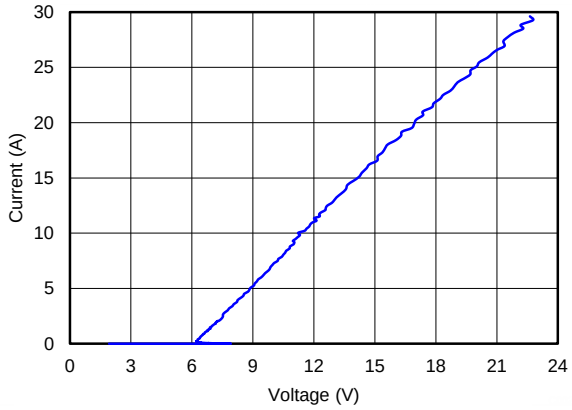


Figure 2. Negative TLP Curve

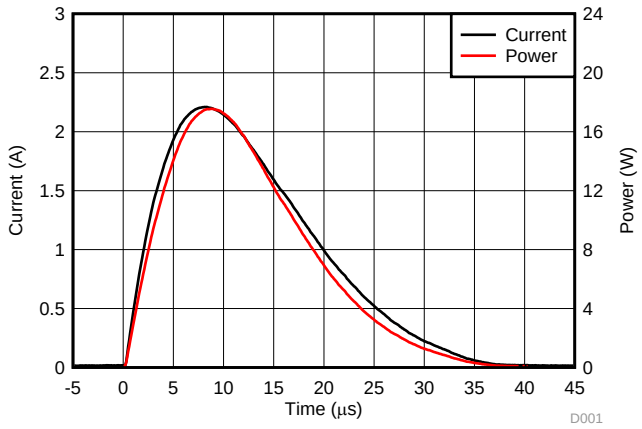


Figure 3. Surge Curve (t_p = 8/20 µs), any IO pin to GND

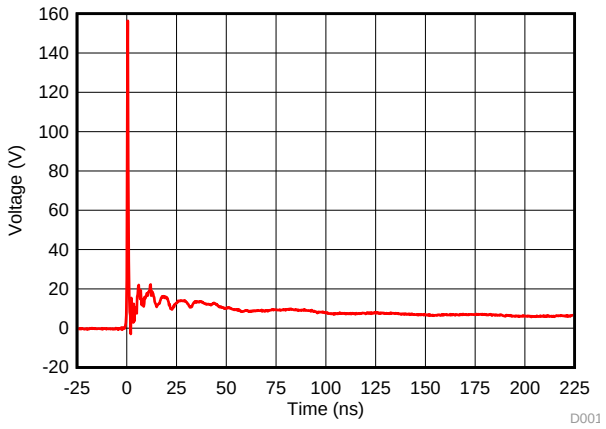


Figure 4. 8-kV IEC Waveform

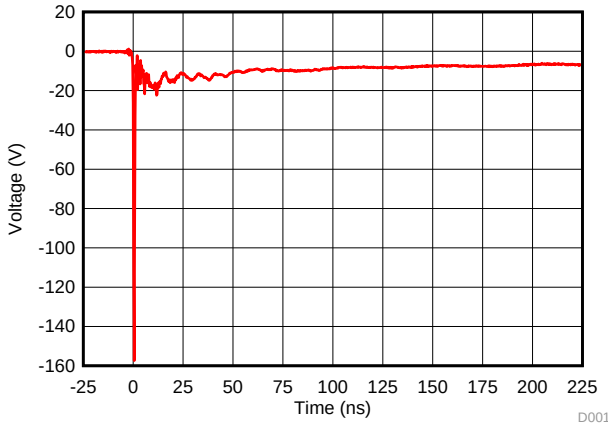


Figure 5. –8-kV IEC Waveform

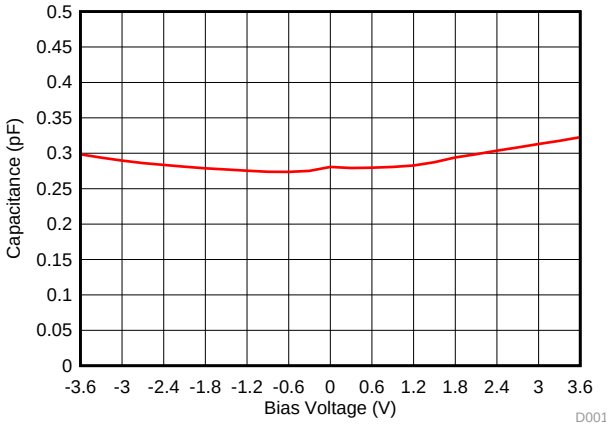


Figure 6. Capacitance vs Bias Voltage

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Typical Characteristics (continued)

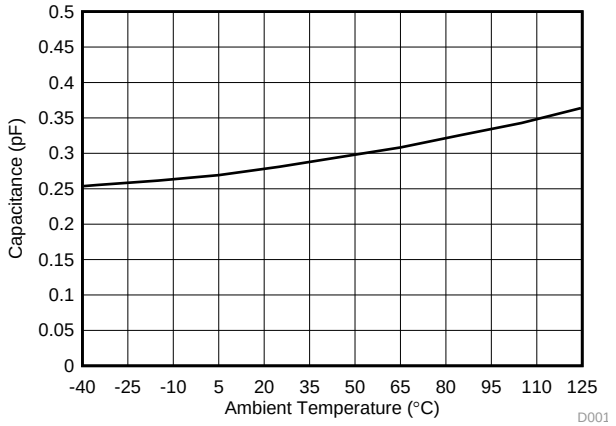


Figure 7. Capacitance vs Ambient Temperature

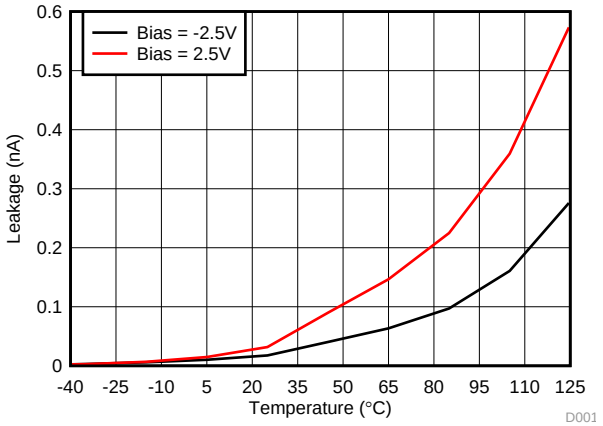


Figure 8. Leakage Current vs Temperature

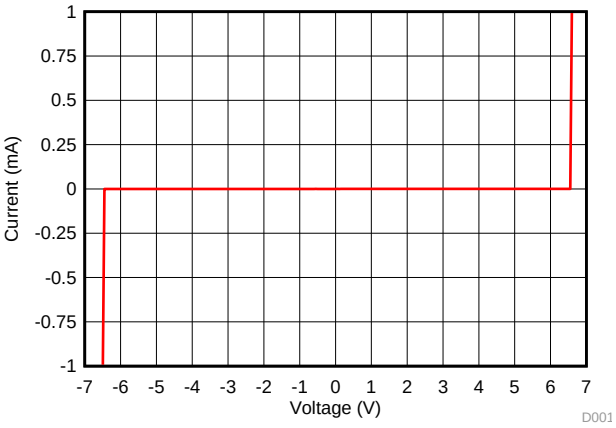


Figure 9. DC Voltage Sweep I-V Curve

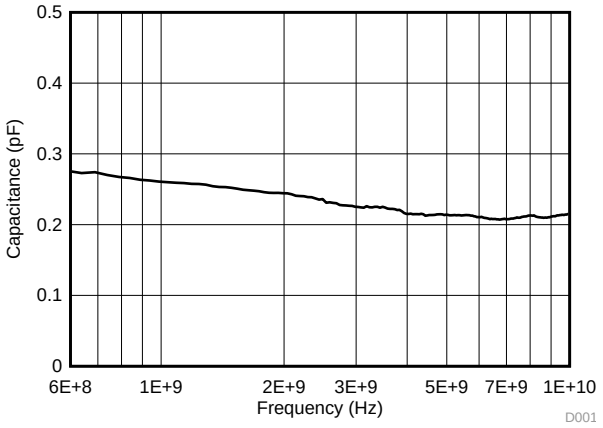


Figure 10. Capacitance vs Frequency

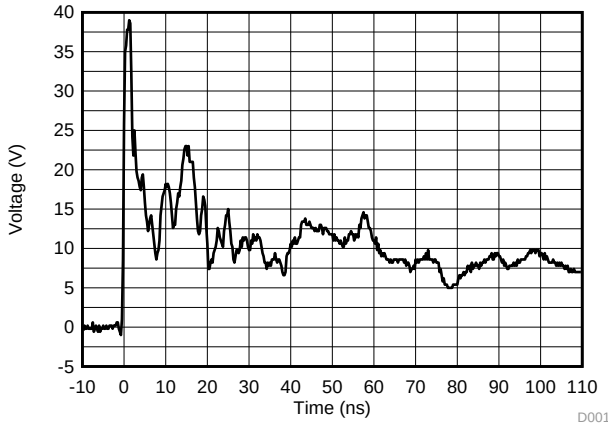


Figure 11. 8-kV IEC Waveform through 2-m HDMI Cable

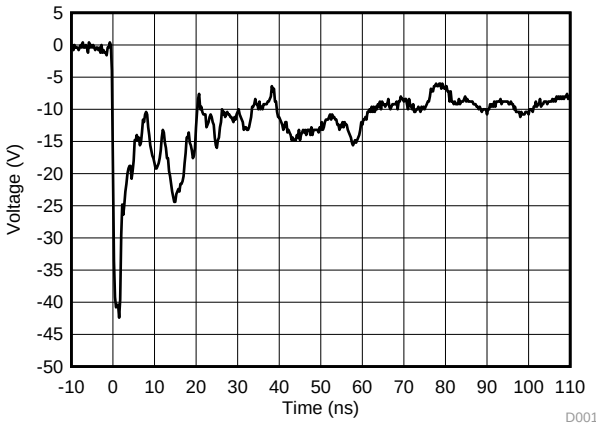


Figure 12. –8-kV IEC Waveform through 2-m HDMI Cable

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Typical Characteristics (continued)

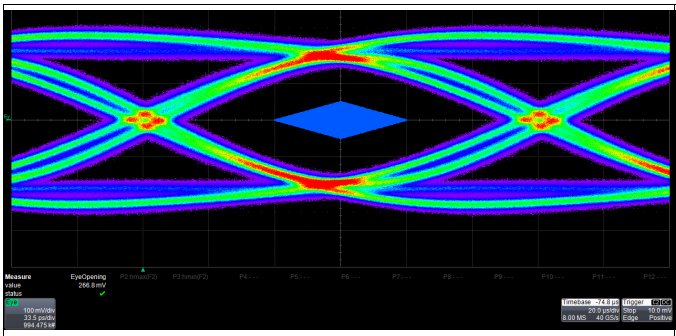


Figure 13. USB3.0 Eye Diagram (Bare Board)

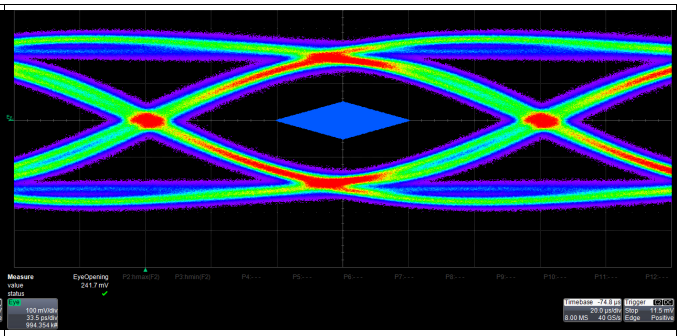


Figure 14. USB3.0 Eye Diagram (With TPD4E02B04)

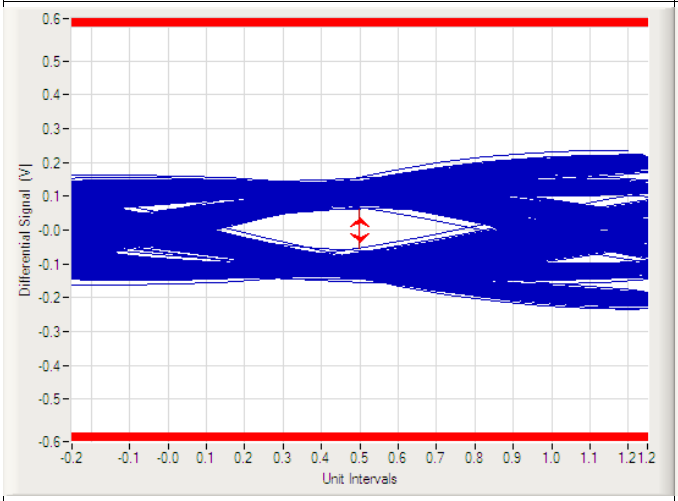


Figure 15. USB3.1 Gen 2 Eye Diagram (Bare Board)

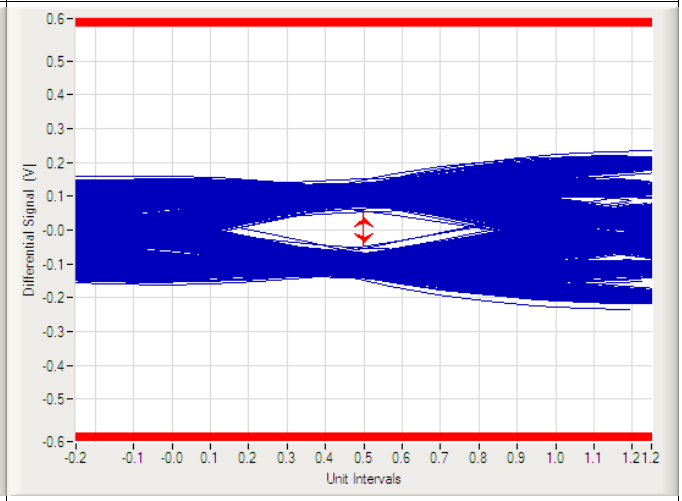


Figure 16. USB3.1 Gen 2 Eye Diagram (With TPD4E02B04)

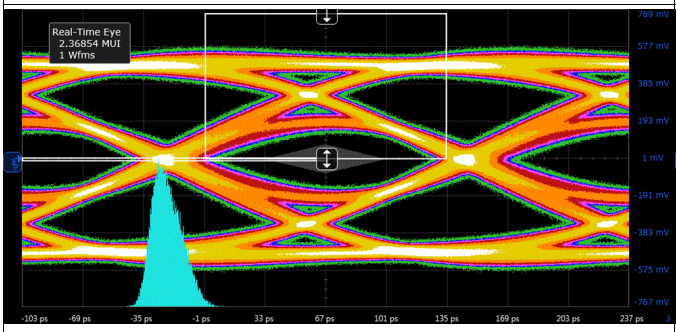


Figure 17. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

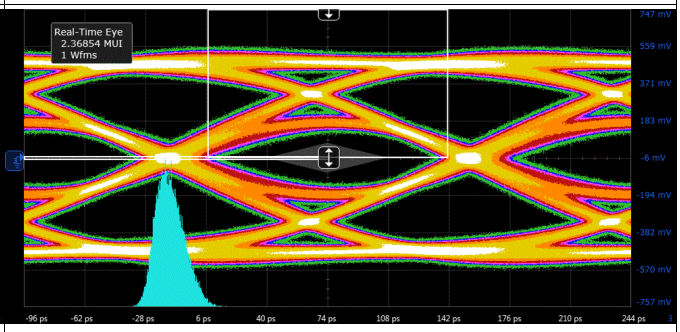


Figure 18. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD4E02B04)

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Typical Characteristics (continued)

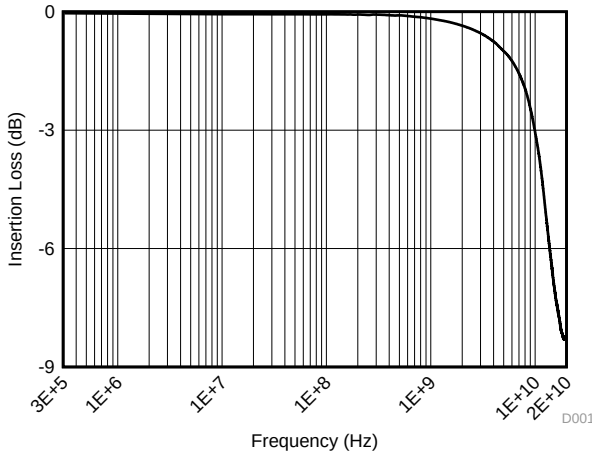


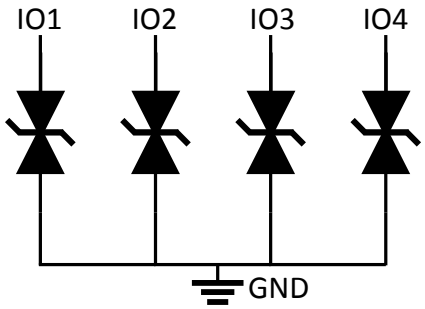
Figure 19. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E02B04 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.25 pF (typical) and 0.33 pF (maximum). This device supports data rates up to 10 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ±5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.8 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps, because of the extremely low IO capacitance.

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Feature Description (continued)

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD4E02B04 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD4E02B04 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E02B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

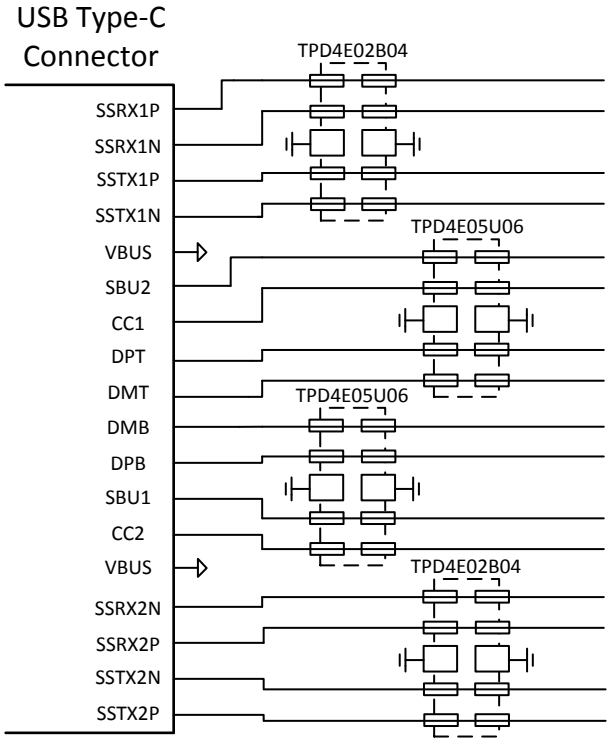


Figure 20. USB 3.1 Gen 2 Type-C ESD Schematic

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Typical Application (continued)

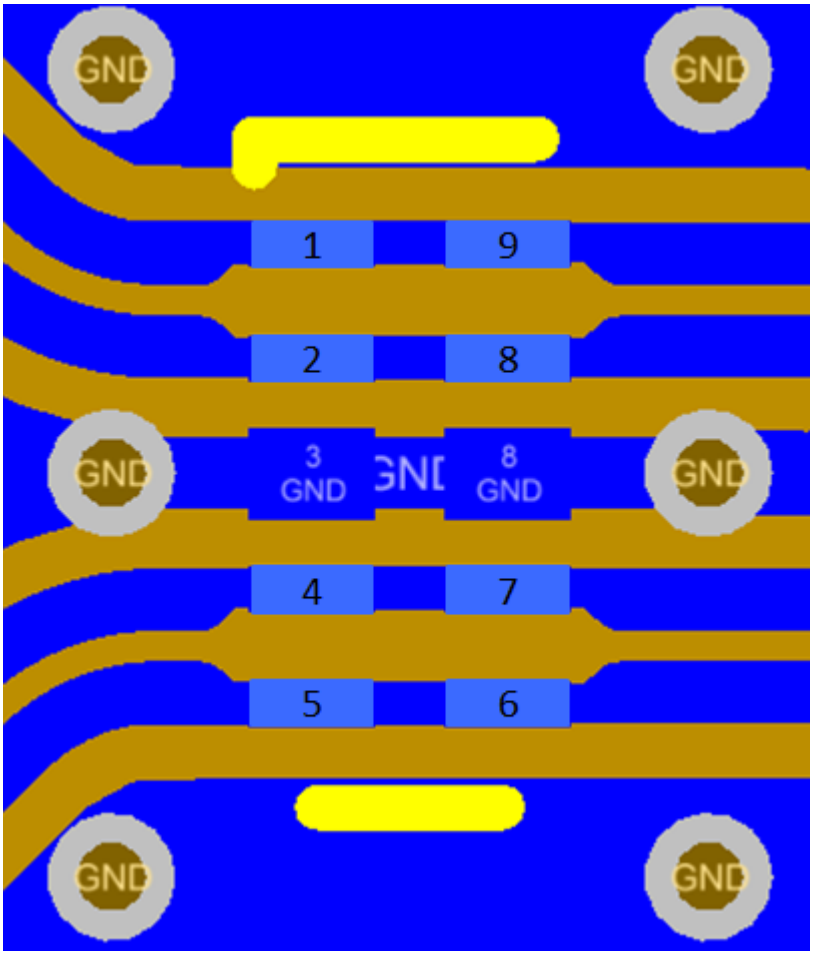


Figure 21. USB 3.1 Gen 2 SuperSpeed Layout

8.2.1 Design Requirements

For this design example two TPD4E02B04 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the USB 3.1 Gen 2 Type-C application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on SuperSpeed+ Lines	0 V to 3.6 V
Operating Frequency on SuperSpeed+ Lines	5 GHz
Signal Range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating Frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD4E02B04 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP/DM lines.

8.2.2.2 Operating Frequency

The TPD4E02B04 has a 0.25 pF (typical) capacitance, which supports the USB3.1 Gen 2 data rates of 10 Gbps. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates.

8.2.3 Application Curves

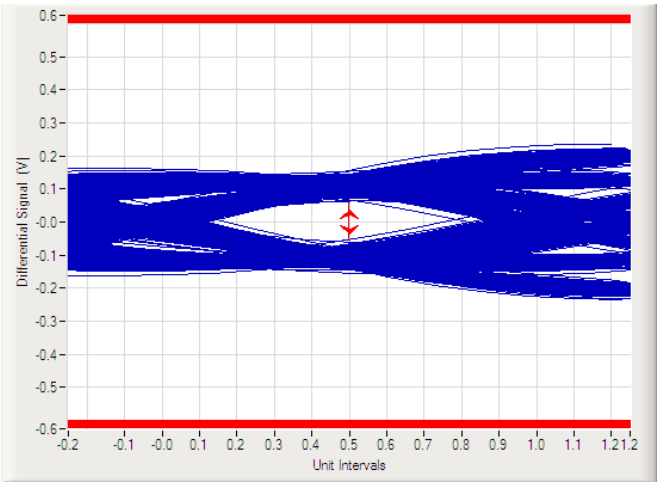


Figure 22. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

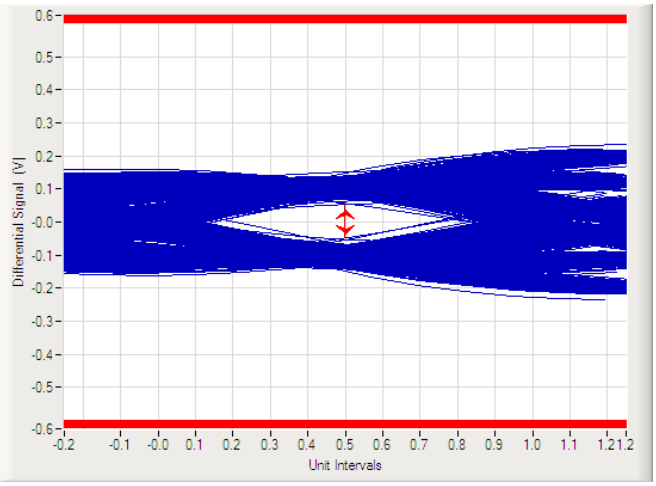


Figure 23. USB 3.1 Gen 2 10-Gbps Eye Diagram (With TPD4E02B04)

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9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

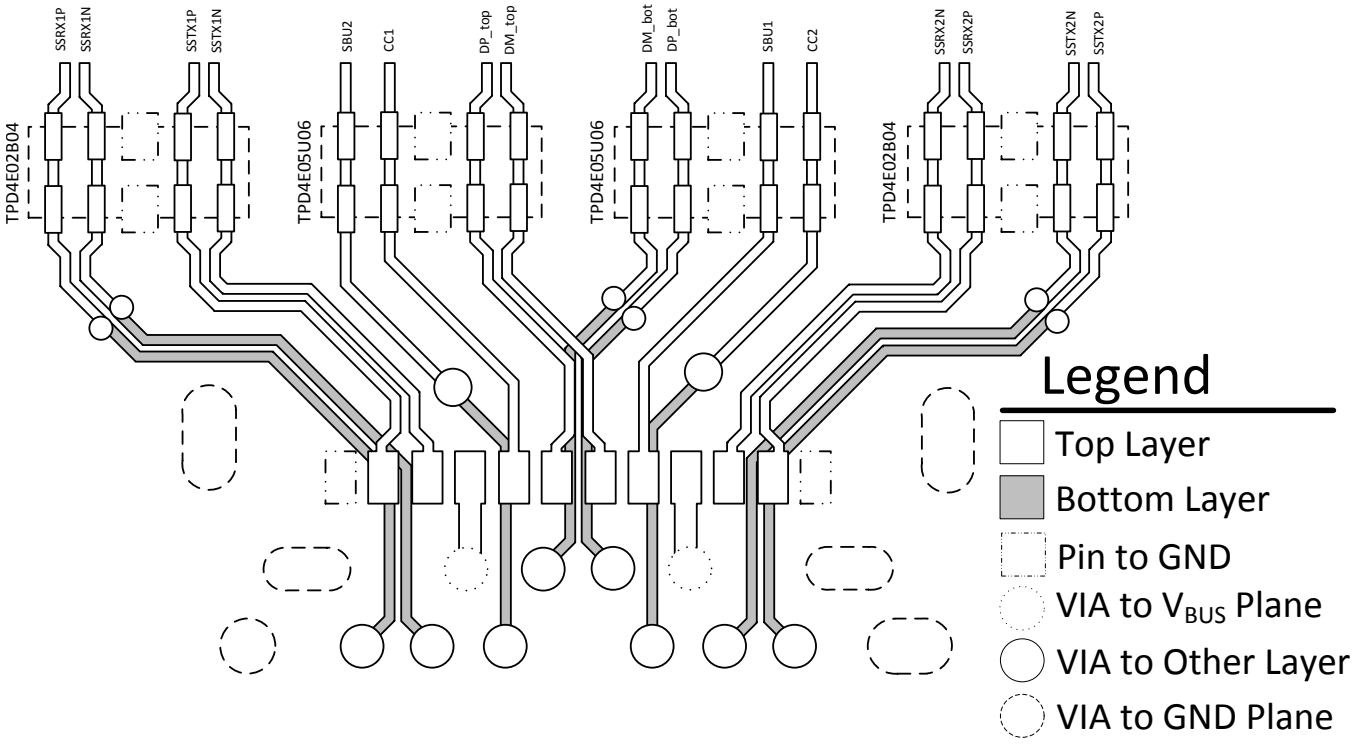


Figure 24. USB Type-C Mid-Mount, Hybrid Connector with One-Sided ESD Layout

Layout Examples (continued)

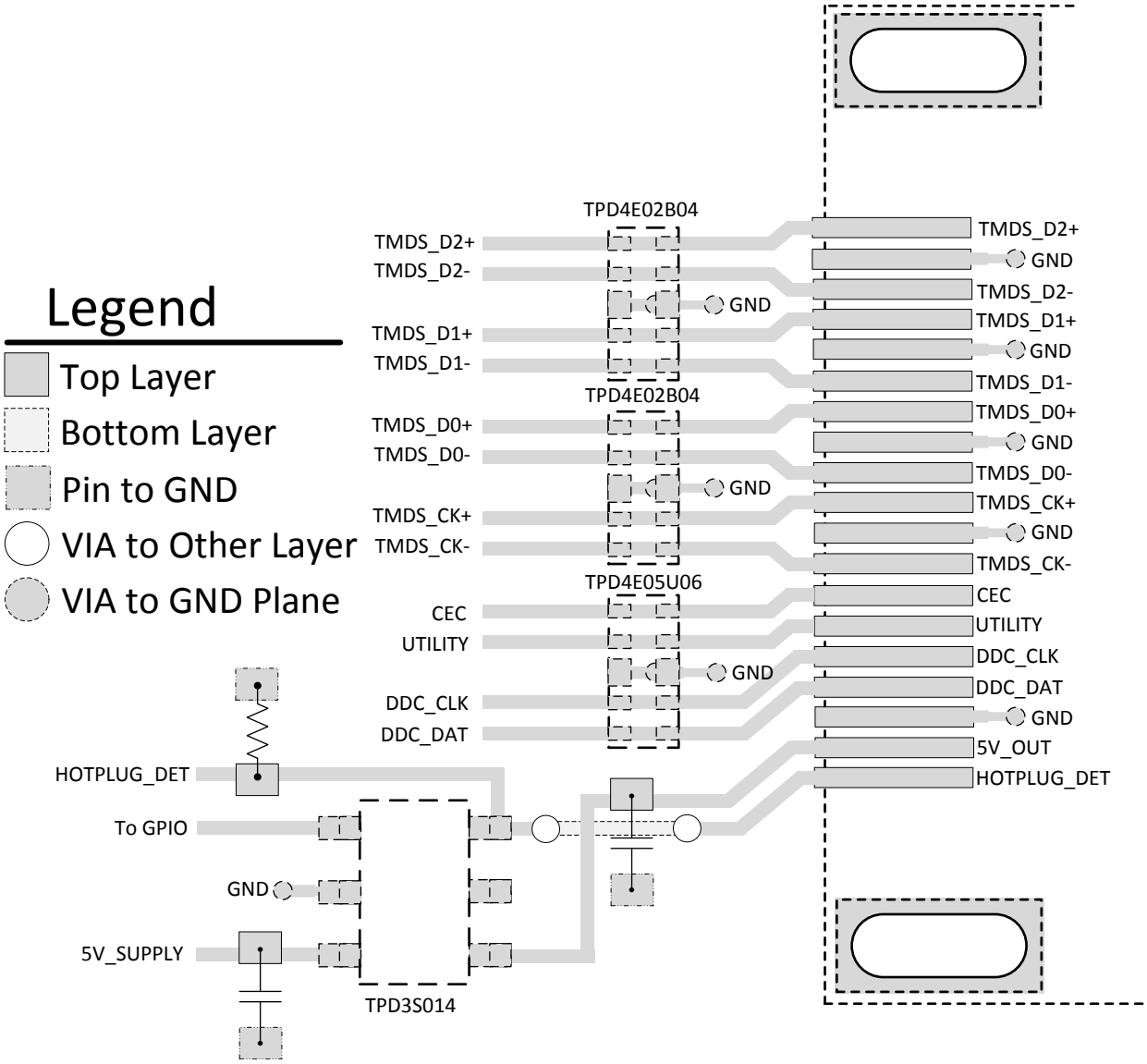


Figure 25. HDMI2.0 Type-A Transmitter Port Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*, SLLA305
- *ESD Layout Guide*, SLVA680
- *Picking ESD Diodes for Ultra High-Speed Data Lines*, SLVA785
- *TPD4E02B04EVM Users Guide*, SLVUAH6

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E02B04DQAR	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQAR.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQARG4.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD4E02B04 :

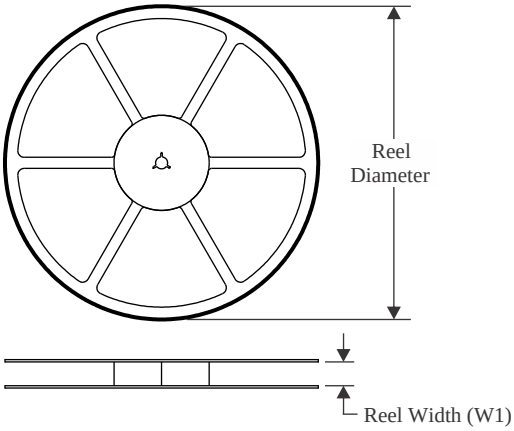
- Automotive : TPD4E02B04-Q1

NOTE: Qualified Version Definitions:

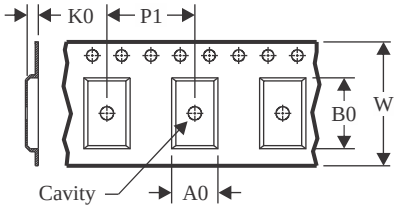
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

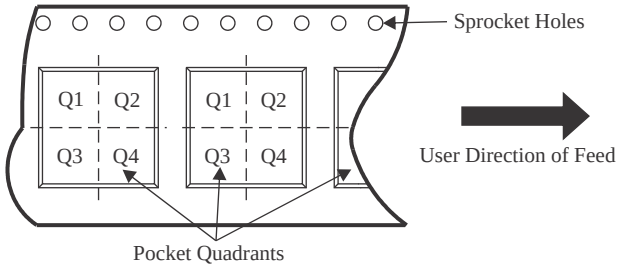


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

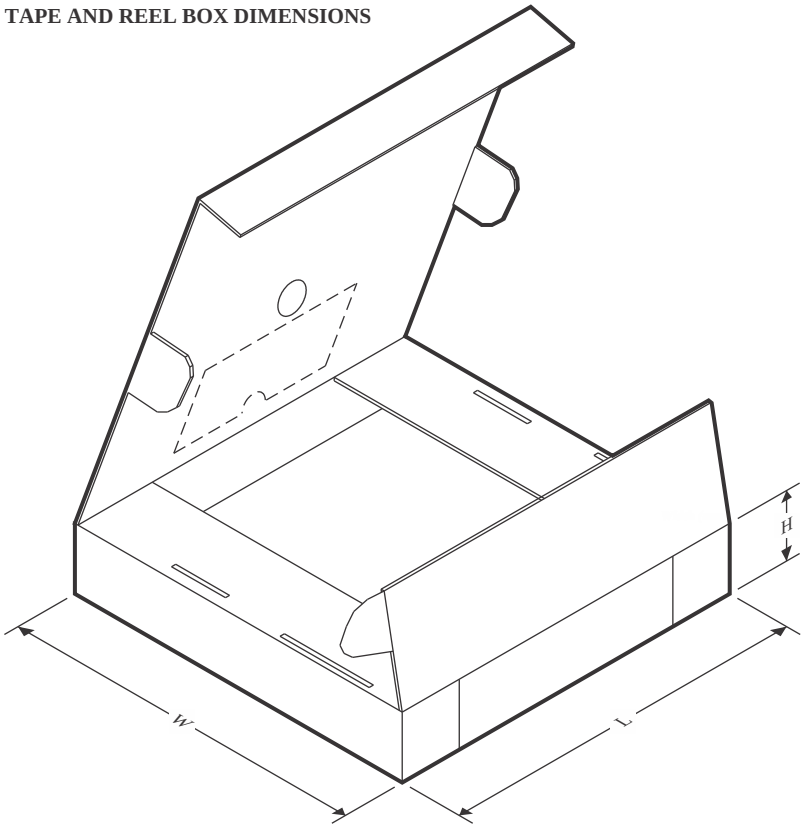
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E02B04DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E02B04DQAR	USON	DQA	10	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

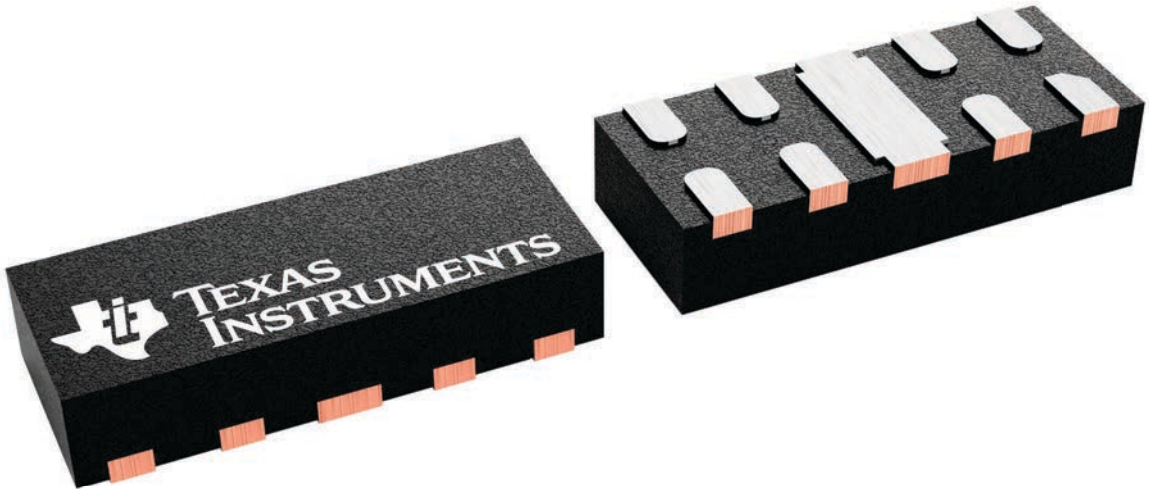
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



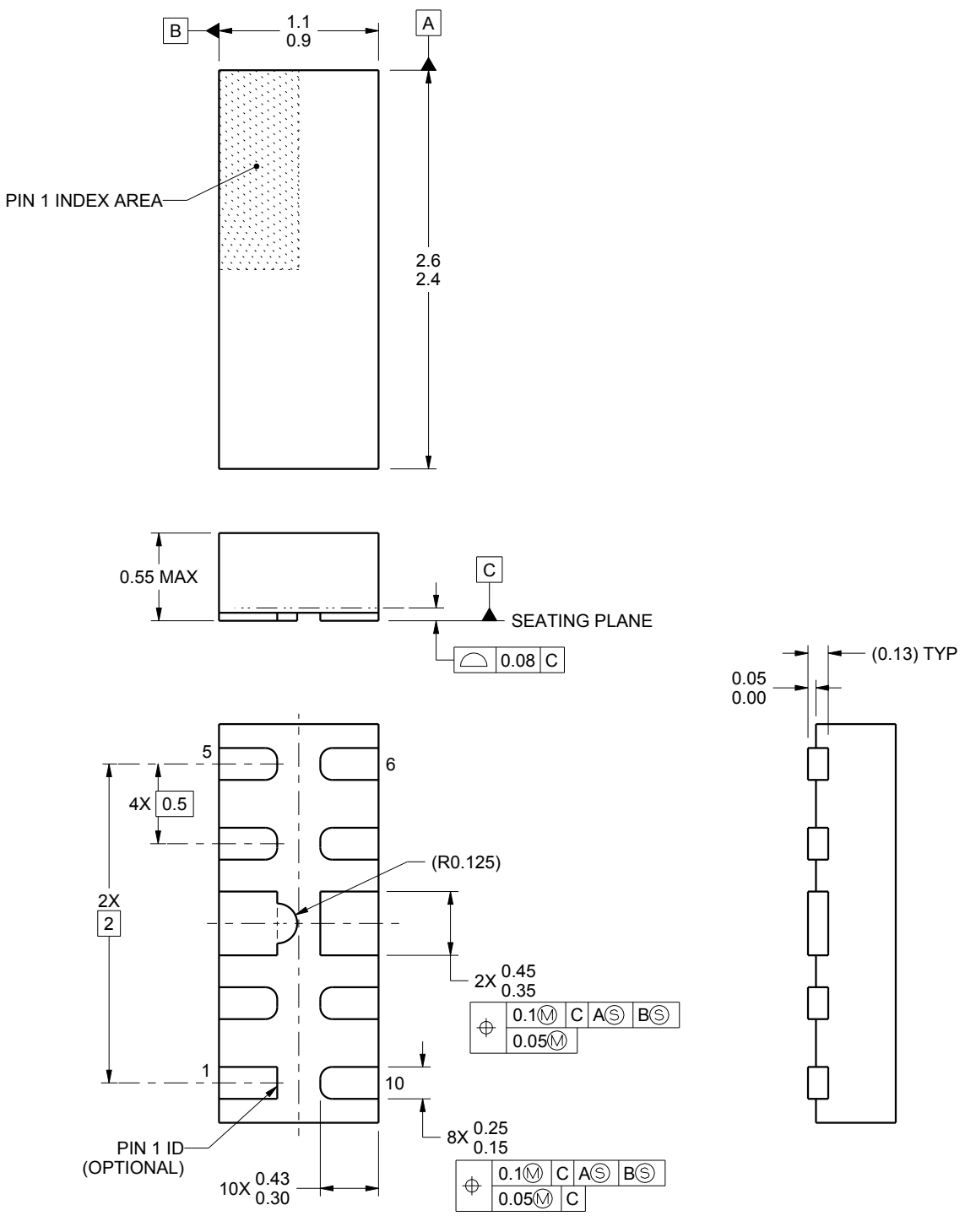
4230320/A

PACKAGE OUTLINE

DQA0010A

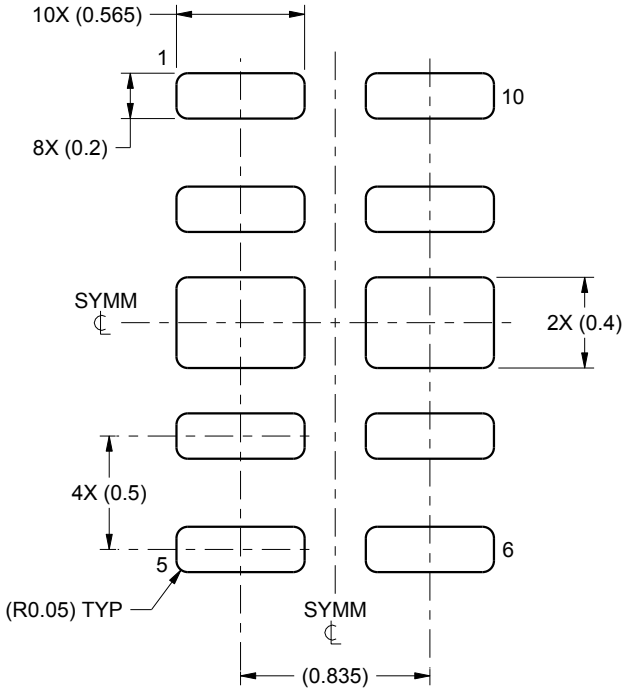
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

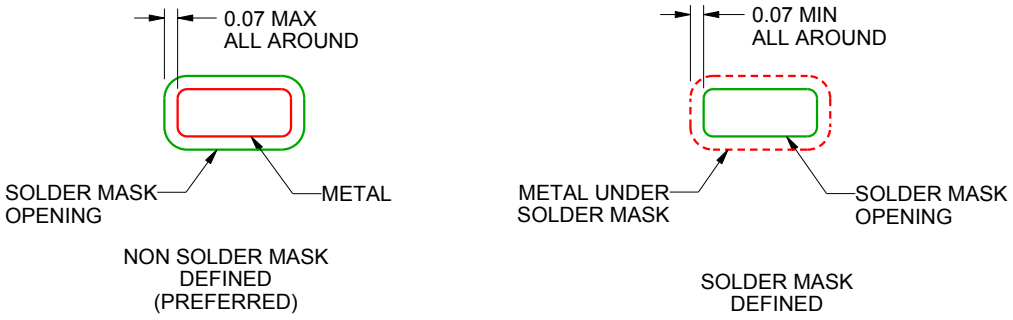


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

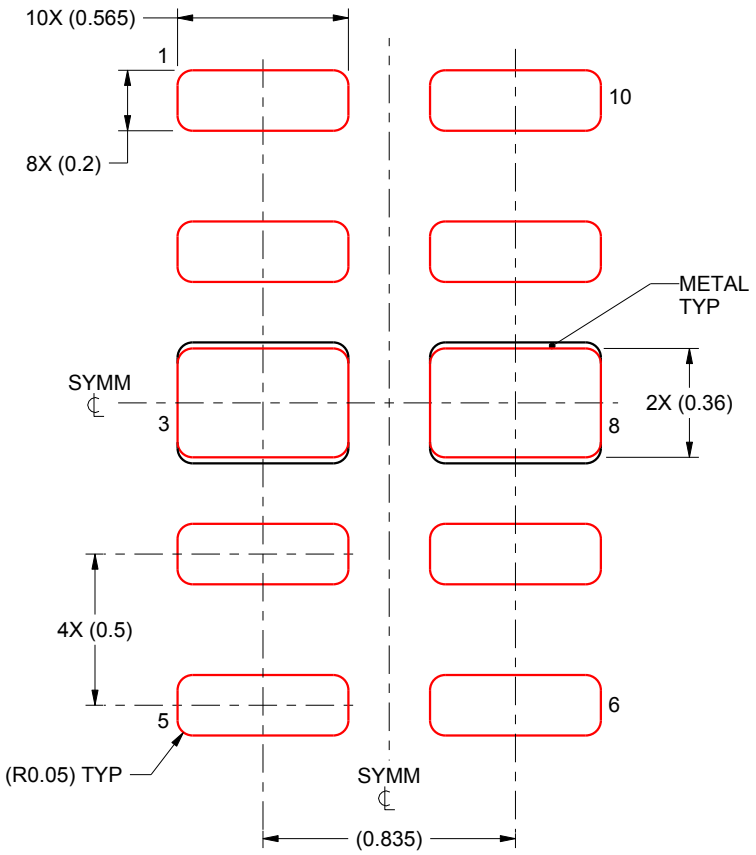
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025

TPS2116 1.6 V to 5.5 V, 2.5-A Low I_Q Power Mux with Manual and Priority Switchover

1 Features

- Input voltage range: 1.6 V to 5.5 V
- Maximum continuous current: 2.5 A
- On-resistance: 40 mΩ (typical)
- VIN2 standby current: 50 nA (typical)
- Quiescent current: 1.32 uA (typical)
- Switchover modes:
  - Priority mode
  - Manual mode
- Controlled output slew rate:
  - 1.3 ms (typical) at 3.3 V
- Reverse Current Blocking when VOUT > VINx
- Thermal shutdown

2 Applications

- Backup battery systems
- E-Meters
- Motor Drives
- Building Automation

3 Description

The TPS2116 is a power mux device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

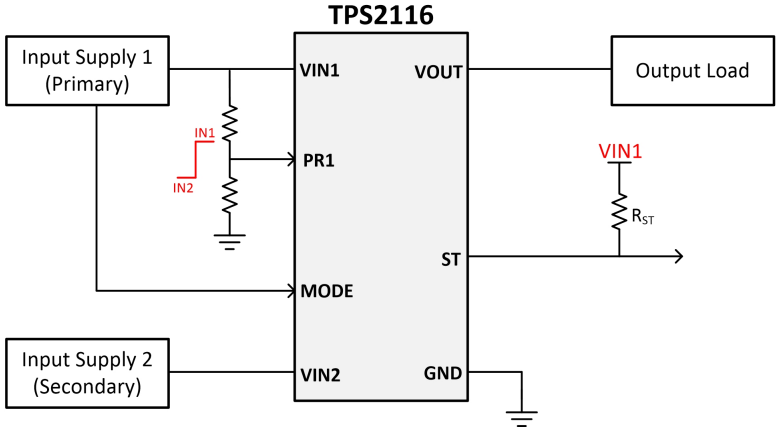
Due to its low quiescent of 1.32 uA (typical) and low standby current of 50 nA (typical), the TPS2116 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

The TPS2116 can be configured for two different switchover behaviors depending on the application. Automatic priority mode prioritizes the supply connected to VIN1 and switches over to the secondary supply (VIN2) when VIN1 drops. Manual mode allows the user to toggle a GPIO or enable signal to switch between channels.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2116	SOT (8)	2.1 mm x 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Basic Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision * (January 2021) to Revision A (May 2021)	Page
• Changed status from "Advance Information" to "Production Data"	1

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5 Pin Configuration and Functions

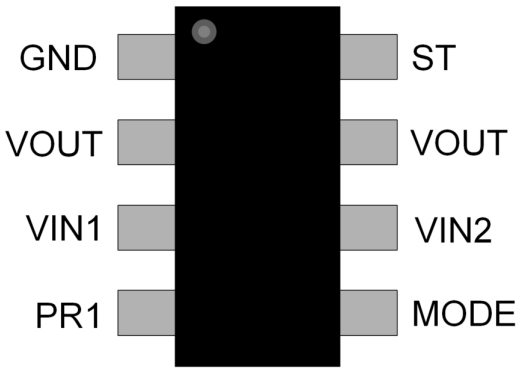


Figure 5-1. DRL Package 8-Pin SOT Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	-	Device ground.
VOUT	2, 7	O	Output power.
VIN1	3	I	Channel 1 input power.
PR1	4	I	Selects between VIN1 and VIN2. When PR1 is high VIN1 is selected, and when PR1 is low VIN2 is selected.
MODE	5	I	Device is put into Priority mode when MODE is tied to VIN1 and manual mode when MODE is pulled up to an external voltage.
VIN2	6	I	Channel 2 input power.
ST	8	O	Open drain status pin. Pulled low when VIN1 is not being used.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN1}, V_{IN2}	Input Voltage	–0.3	6	V
V_{OUT}	Output Voltage	–0.3	6	V
V_{ST}, V_{PR1}, V_{MODE}	Control Pin Voltage	–0.3	6	V
I_{MAX}	Maximum Current		2.5	A
$I_{MAX,PLS}$	Maximum Pulsed Current Max duration 1ms, Duty cycle of 2%		4	A
T_J	Junction temperature		Internally Limited	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}, V_{IN2}	Input Voltage	1.6		5.5	V
V_{OUT}	Output Voltage	0		5.5	V
V_{ST}, V_{MODE}, V_{PR1}	Control Pin Voltage	0		5.5	V
T_A	Ambient Temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS2116 DRL (SOT) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.1	°C/W

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6.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS2116 DRL (SOT) 8-PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{STBY, VIN1}$	VIN1 Standby Current	VIN2 powers VOUT VIN1 > VIN2 + 0.1V	25°C		1.1		uA
			-40°C to 85°C			1.9	uA
			-40°C to 105°C			2	uA
		VIN2 powers VOUT VIN2 > VIN1 + 0.2V	25°C		0.22		uA
			-40°C to 85°C			0.31	uA
			-40°C to 105°C			0.32	uA
$I_{STBY, VIN2}$	VIN2 Standby Current	VIN1 powers VOUT VIN2 > VIN1 + 0.2V	25°C		1.2		uA
			-40°C to 85°C			2	uA
			-40°C to 105°C			2.1	uA
		VIN1 powers VOUT VIN1 > VIN2 + 0.1V	25°C		0.05		uA
			-40°C to 85°C			0.07	uA
			-40°C to 105°C			0.09	uA
$I_{Q, VIN1}$	VIN1 Quiescent Current	VIN1 powers VOUT VIN1 > VIN2 + 0.1V	25°C		1.32		uA
			-40°C to 85°C			3.6	uA
			-40°C to 105°C			4.4	uA
		VIN1 powers VOUT VIN2 > VIN1 + 0.2V	25°C		0.3		uA
			-40°C to 85°C			0.51	uA
			-40°C to 105°C			0.55	uA
$I_{Q, VIN2}$	VIN2 Quiescent Current	VIN2 powers VOUT VIN2 > VIN1 + 0.2V	25°C		1.35		uA
			-40°C to 85°C			3.7	uA
			-40°C to 105°C			4.5	uA
		VIN2 powers VOUT VIN1 > VIN2 + 0.1V	25°C		0.1		uA
			-40°C to 85°C			0.27	uA
			-40°C to 105°C			0.29	uA
$I_{SD,VIN1}$	VIN1 Shutdown Current	MODE = 0V, PR1 = 5V VIN1 > VIN2 VOUT = 0V	25°C		0.1		uA
			-40°C to 85°C			1.3	uA
			-40°C to 105°C			2.9	uA
		MODE = 0V, PR1 = 5V VIN1 < VIN2 VOUT = 0V	25°C		0.05		uA
			-40°C to 85°C			1	uA
			-40°C to 105°C			2.4	uA

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SD,VIN2}$	VIN2 Shutdown Current	MODE = 0V, PR1 = 5V VIN2 > VIN1 VOUT = 0V	25°C		0.05		uA
			-40°C to 85°C			1.3	uA
			-40°C to 105°C			2.9	uA
		MODE = 0V, PR1 = 5V VIN2 < VIN1 VOUT = 0V	25°C		0.05		uA
			-40°C to 85°C			0.7	uA
			-40°C to 105°C			2.1	uA
I_{REV}	Reverse leakage current out of VINx	V_{OUT} = 5.5V V_{INx} = 0V, V_{INy} = Open	25°C		0.001		uA
			85°C		0.05		uA
			105°C		0.15		uA
	Reverse leakage current into VOUT	V_{OUT} = 5.5V V_{INx} = 0V, V_{INy} = Open	25°C		0.01		uA
			85°C		0.1		uA
			105°C		0.25		uA
I_{PR1}	PR1 pin leakage		-40°C to 105°C			0.1	uA
I_{MODE}	MODE pin leakage		-40°C to 105°C			0.1	uA
I_{ST}	ST pin leakage		-40°C to 105°C			0.03	uA
Performance							
R_{ON}	On-Resistance	VINx = 5V I_{OUT} = 200mA	25°C		37	46	mΩ
			-40°C to 85°C			55	mΩ
			-40°C to 105°C			60	mΩ
		VINx = 3.3V I_{OUT} = 200mA	25°C		40	48	mΩ
			-40°C to 85°C			55	mΩ
			-40°C to 105°C			59	mΩ
		VINx = 1.8V I_{OUT} = 200mA	25°C		41	51	mΩ
			-40°C to 85°C			61	mΩ
			-40°C to 105°C			66	mΩ
		VINx = 1.6V I_{OUT} = 200mA	25°C		42	52	mΩ
			-40°C to 85°C			68	mΩ
			-40°C to 105°C			74	mΩ
$V_{OL,ST}$	Status pin V_{OL}	I_{ST} = 1mA	-40°C to 105°C			0.1	V
t_{ST}	Status pin response time	ST pin pulled high to low R_{ST} = 10kΩ	-40°C to 105°C		5		us
V_{REF}	PR1 reference voltage		-40°C to 105°C	0.92	1	1.08	V
$V_{IH,MODE}$	MODE logic high threshold		-40°C to 105°C	1		5.5	V
$V_{IL,MODE}$	MODE logic low threshold		-40°C to 105°C	0		0.35	V
Protection							
t_{RCB}	Reverse current blocking response time	VOUT > Selected VIN + 1V	-40°C to 105°C		2		us
$V_{RCB,R}$	Reverse current blocking rising threshold (V_{OUT} - V_{IN})		-40°C to 105°C		42	70	mV
$V_{RCB,F}$	Reverse current blocking falling threshold (V_{OUT} - V_{IN})		-40°C to 105°C		17	40	mV
I_{RCB}	Reverse current blocking activation current		-40°C to 105°C		1.4	4	A
TSD	Thermal shutdown		-		170		°C

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
TSD_{HYS}	Thermal shutdown hysteresis		-		20		°C

6.6 Switching Characteristics

Typical switching characteristics are defined at an ambient temperature of 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switchover						
t_{SW}	Switchover time, VINx = 5 V	R_L = 10 Ω, C_L = 10 uF		8		us
t_{SW}	Switchover time, VINx = 3.3 V	R_L = 10 Ω, C_L = 10 uF		6.2		us
t_{SW}	Switchover time, VINx = 1.8 V	R_L = 10 Ω, C_L = 10 uF		17.7		us
t_D	Delay time, VINx = 5 V	R_L = 100 Ω, C_L = 10 uF		1		ms
t_D	Delay time, VINx = 3.3 V	R_L = 100 Ω, C_L = 10 uF		1.2		ms
t_D	Delay time, VINx = 1.8 V	R_L = 100 Ω, C_L = 10 uF		1.4		ms
t_{SS}	Soft-start time, VINx = 5 V	R_L = 100 Ω, C_L = 10 uF		1.7		ms
t_{SS}	Soft-start time, VINx = 3.3 V	R_L = 100 Ω, C_L = 10 uF		1.3		ms
t_{SS}	Soft-start time, VINx = 1.8 V	R_L = 100 Ω, C_L = 10 uF		0.9		ms

6.7 Timing Diagrams

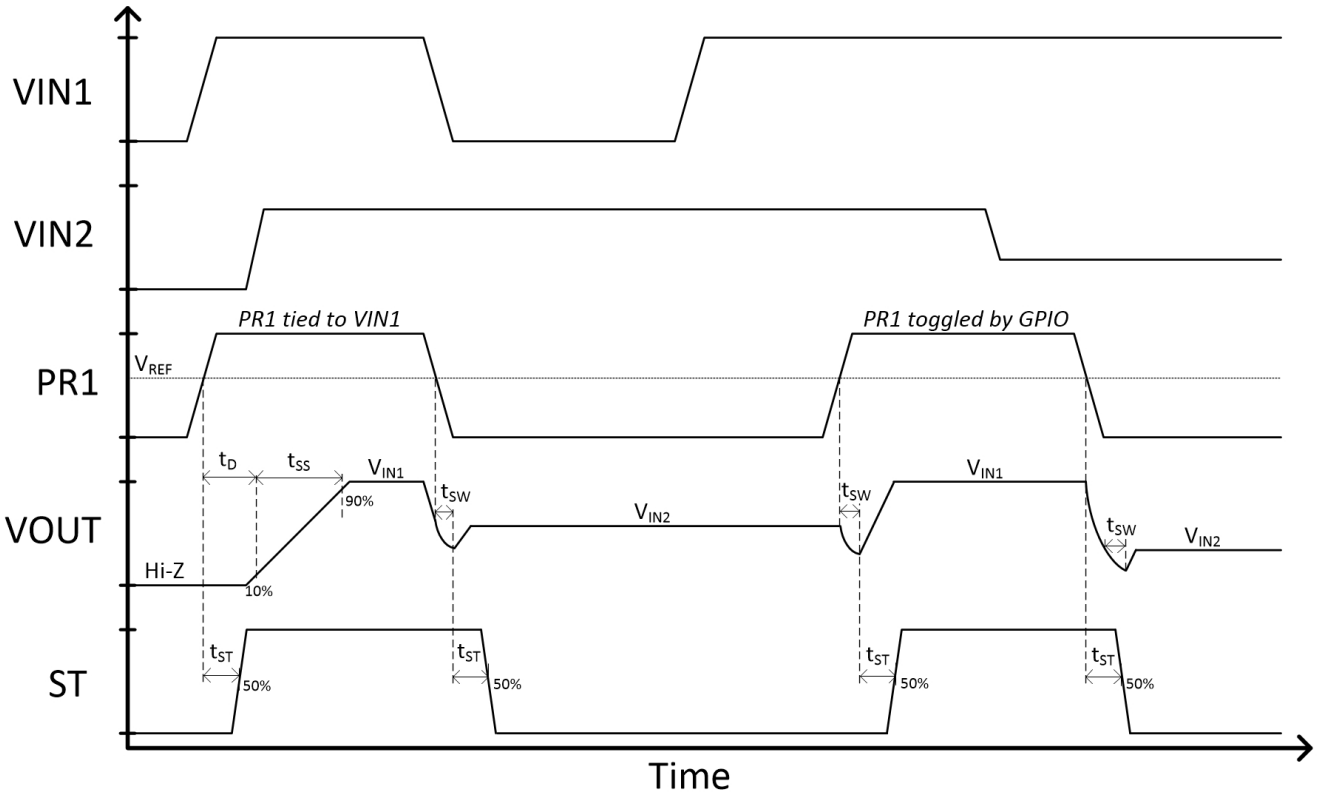
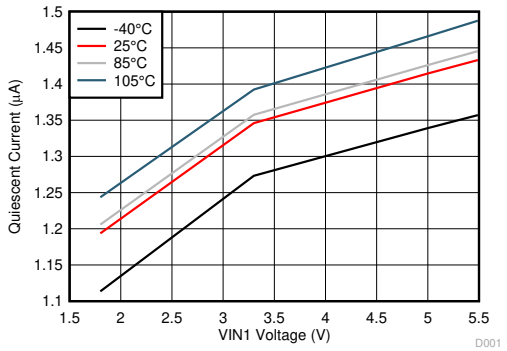


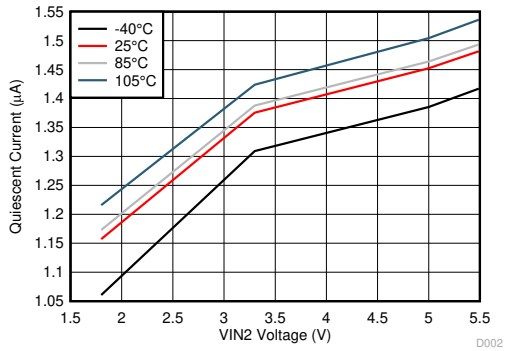
Figure 6-1. TPS2116 Timing Diagram

6.8 Typical Characteristics



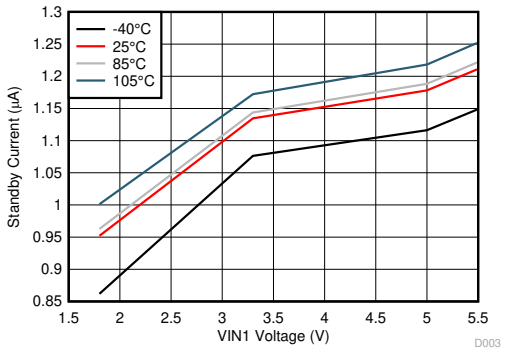
VIN2 = 1.6 V VOUT = Open

Figure 6-2. VIN1 Quiescent Current vs Input Voltage



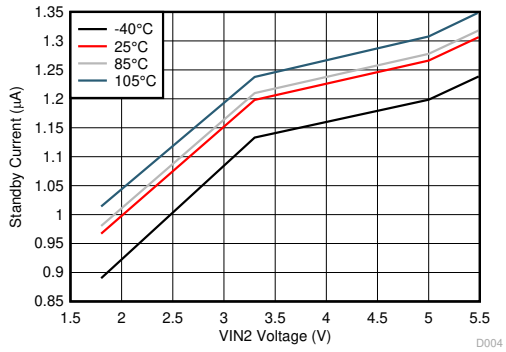
VIN1 = 1.6 V VOUT = Open

Figure 6-3. VIN2 Quiescent Current vs Input Voltage



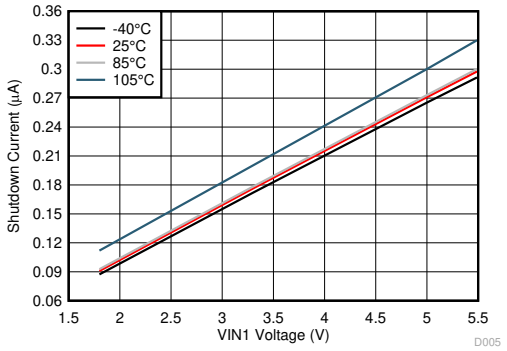
VIN2 = 1.6 V VOUT = Open

Figure 6-4. VIN1 Standby Current vs Input Voltage



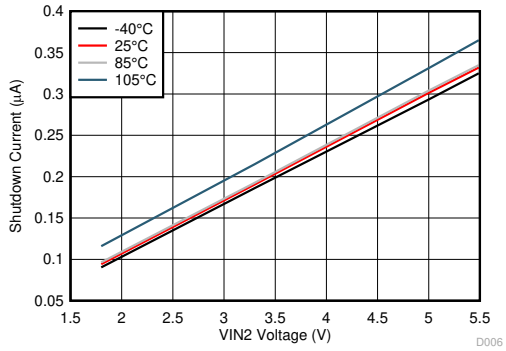
VIN1 = 1.6 V VOUT = Open

Figure 6-5. VIN2 Standby Current vs Input Voltage



VIN2 = 1.6 V VOUT = Open

Figure 6-6. VIN1 Shutdown Current vs Input Voltage

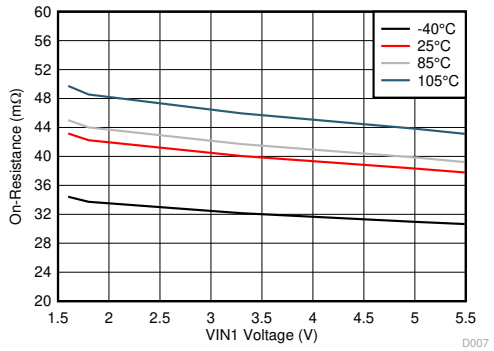


VIN1 = 1.6 V VOUT = 0 V

Figure 6-7. VIN2 Shutdown Current vs Input Voltage

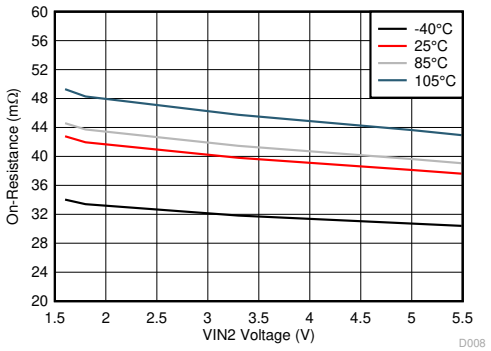
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6.8 Typical Characteristics (continued)



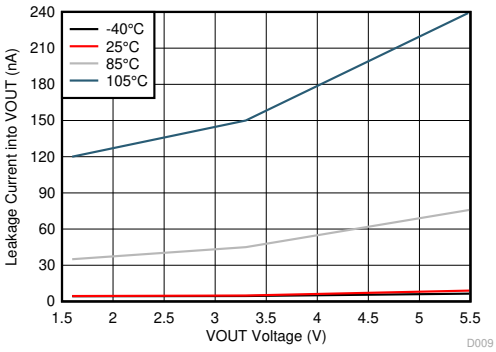
I_{OUT} = 200 mA

Figure 6-8. Channel 1 On-Resistance vs Input Voltage



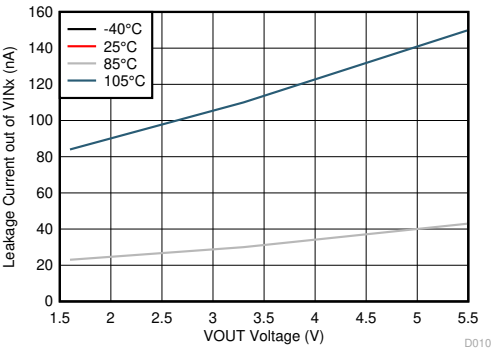
I_{OUT} = 200 mA

Figure 6-9. Channel 2 On-Resistance vs Input Voltage



V_{INx} = 0 V V_{INy} = Open

Figure 6-10. Reverse Leakage Current into VOUT



V_{INx} = 0 V V_{INy} = Open

Figure 6-11. Reverse Leakage Current out of VINx

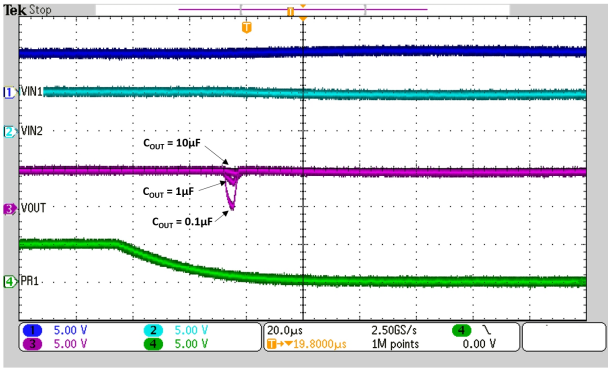


Figure 6-12. Output Voltage Drop vs Output Capacitance (MODE = 5 V, R_L = 10 Ω)

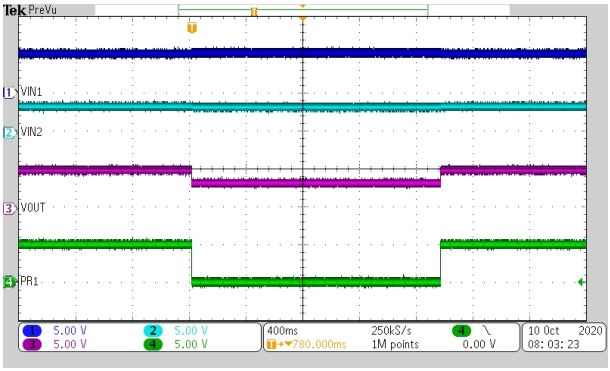


Figure 6-13. Manual Mode Switchover Behavior (MODE = 5 V, R_L = 10 Ω, CL = 10 uF)

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7 Detailed Description

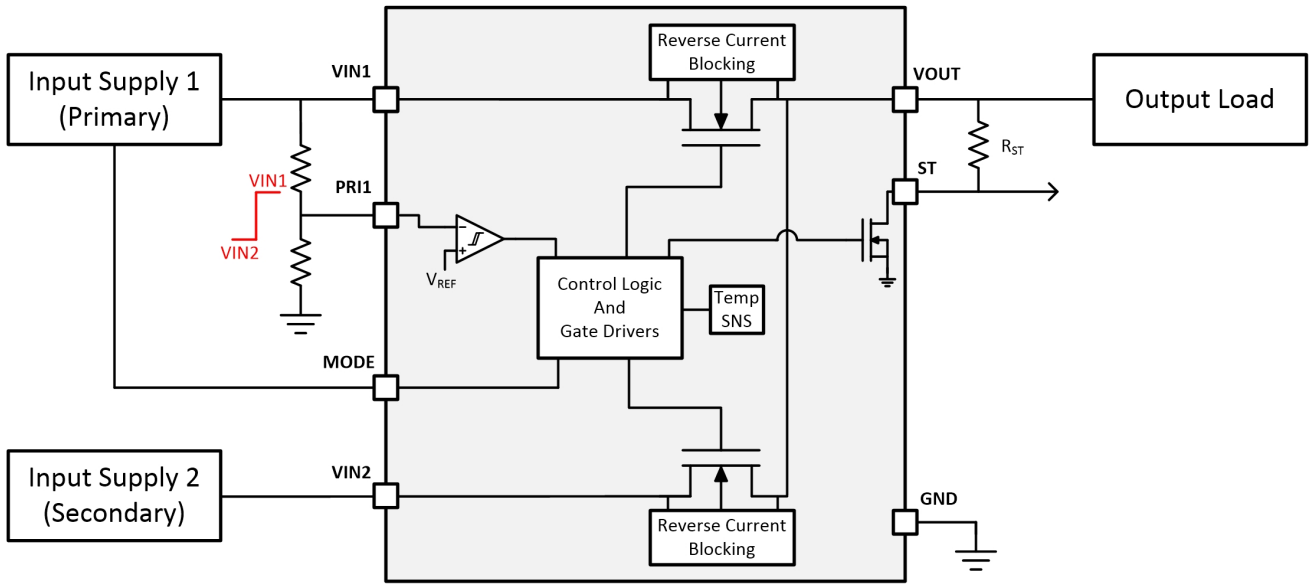
7.1 Overview

The TPS2116 is a power mux device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

The TPS2116 can be configured for two different switchover behaviors depending on the application. Automatic priority mode prioritizes the supply connected to VIN1 and switches over to the secondary supply (VIN2) when VIN1 drops. Manual mode allows the user to toggle a GPIO or enable signal to switch between channels.

Due to its low quiescent of 1.32 uA (typical) and standby current of 50 nA (typical), the TPS2116 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

7.2 Functional Block Diagram



7.3 Feature Description

The below sections detail the features of the TPS2116.

7.3.1 Truth Table

The below table shows the expected behavior of the TPS2116. For Priority mode, VIN1 is connected to PR1 through a resistor divider.

MODE	VIN1	VIN2	PR1	ST	VOUT
VIN1 (Priority mode)	High ($V_{PR1} > V_{REF}$)	X	VIN1 through resistor divider	High	VIN1
	Low ($V_{PR1} < V_{REF}$)	≥ 1.6 V		Low	VIN2
External Bias ≥ 1 V (Manual mode)	≥ 1.6 V	X	High	High	VIN1
	X	≥ 1.6 V	Low	Low	VIN2
External Bias ≤ 0.35 V (Manual mode)	X	X	High	Low	Hi-Z
	> V_{IN2}	X	Low	High	VIN1
	X	> V_{IN1}	Low	Low	VIN2

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X = do not care

7.3.2 Soft Start

When an input voltage is applied to the TPS2116 and the output voltage is lower than 1 V, the output will be brought up with soft start to minimize the inrush current due to output capacitance. However, when the device switches from one power supply to another (switchover) and VOUT > 1 V, soft start is not used to minimize the output voltage drop. For linear soft start behavior, it is recommended to have an output capacitance of at least 0.1 µF.

7.3.3 Status Indication

The ST pin is an open drain output that should be pulled up to an external voltage for proper operation. When the TPS2116 is powering the output using VIN1, the ST pin will be pulled high by the external voltage source. Even if the device is blocking reverse current from VOUT to VIN1, selection of VIN1 will keep the ST pin pulled high. When the TPS2116 is powering the output using VIN2 or both channels are disabled, the ST pin will be pulled low. During thermal shutdown, the ST pin will be pulled low regardless of the channel being used.

7.3.4 Reverse Current Blocking

The TPS2116 initiates reverse current blocking (RCB) when the VOUT voltage is externally biased and exceeds the input voltage supply being used. Once the output voltage is higher than the input voltage by 42mV ($V_{RCB,R}$), the device will shut off. During this state, the leakage into VOUT and out of VIN is defined by I_{REV}. Once the voltage difference between the output and input lowers to 17mV ($V_{RCB,F}$), the channel will turn back on.

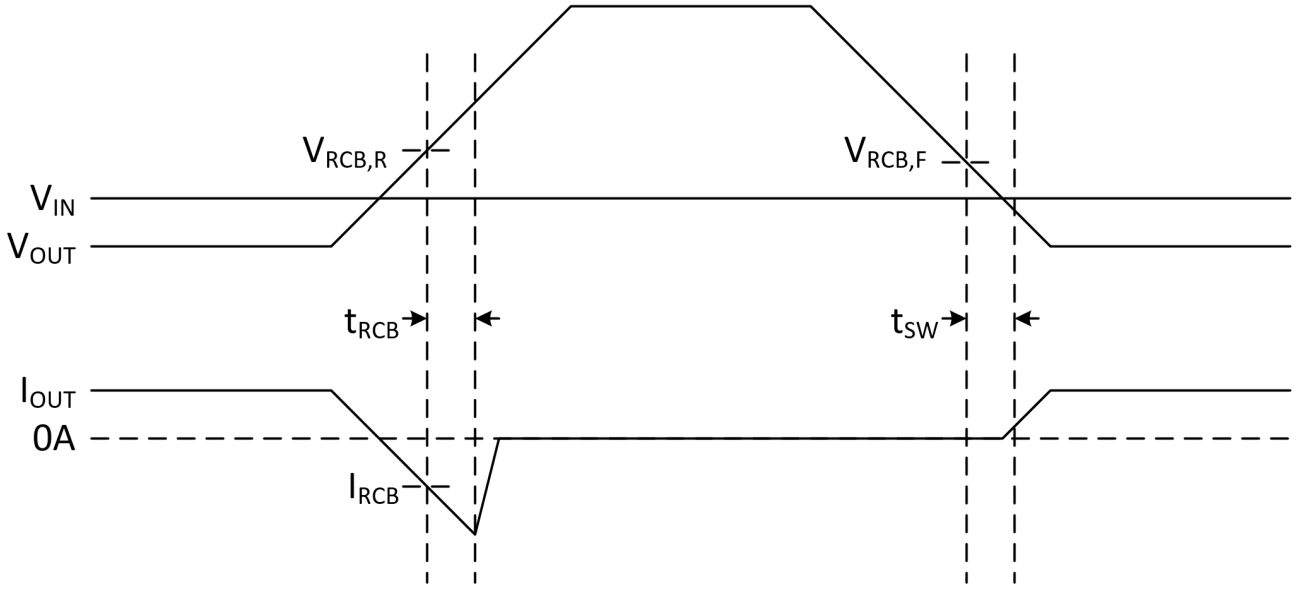


Figure 7-1. Reverse Current Blocking Behavior

If RCB is expected to occur, it is recommended to clamp the output or use a high output capacitance (about 100µF). This will prevent voltage spikes from damaging the device due to output inductance.

7.4 VINx Collapse Rate

The TPS2116 uses the highest voltage supply to power the device. When one supply drops below the other, the device changes the supply used to power the device. If the supply powering the device drops at a rate faster than 1 V/10 µs, the other supply must be at 2.5 V or higher to prevent the device from resetting. If the other supply is lower than 2.5 V, then the device may not be able to switch to the supply quickly enough, and the device will reset and turn on with soft start timing if VOUT < 1 V.

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7.5 Output Voltage Drop

The output voltage drop during switchover from one supply to another is based on the load capacitance and load resistance. The stronger the resistive load, the faster the output will discharge. The higher the capacitance on the output, the less the voltage will drop during switchover.

7.6 Device Functional Modes

The below sections detail the two different configuraiton options for the device.

7.6.1 Priority/Manual Mode

When MODE is tied high, PR1 determines the channel selected. To configure VIN1 as the priority supply, connect MODE to VIN1 and set the proper threshold through a resistor divider from VIN1 to PR1. To configure manual selection, pull up MODE to an external supply and follow the truth table. When PR1 is pulled above V_{REF}, the voltage on VIN1 is used to power the output, and when it is pulled below V_{REF}, VIN2 is used to power the output. The expected behavior for the device is shown in the waveform below.

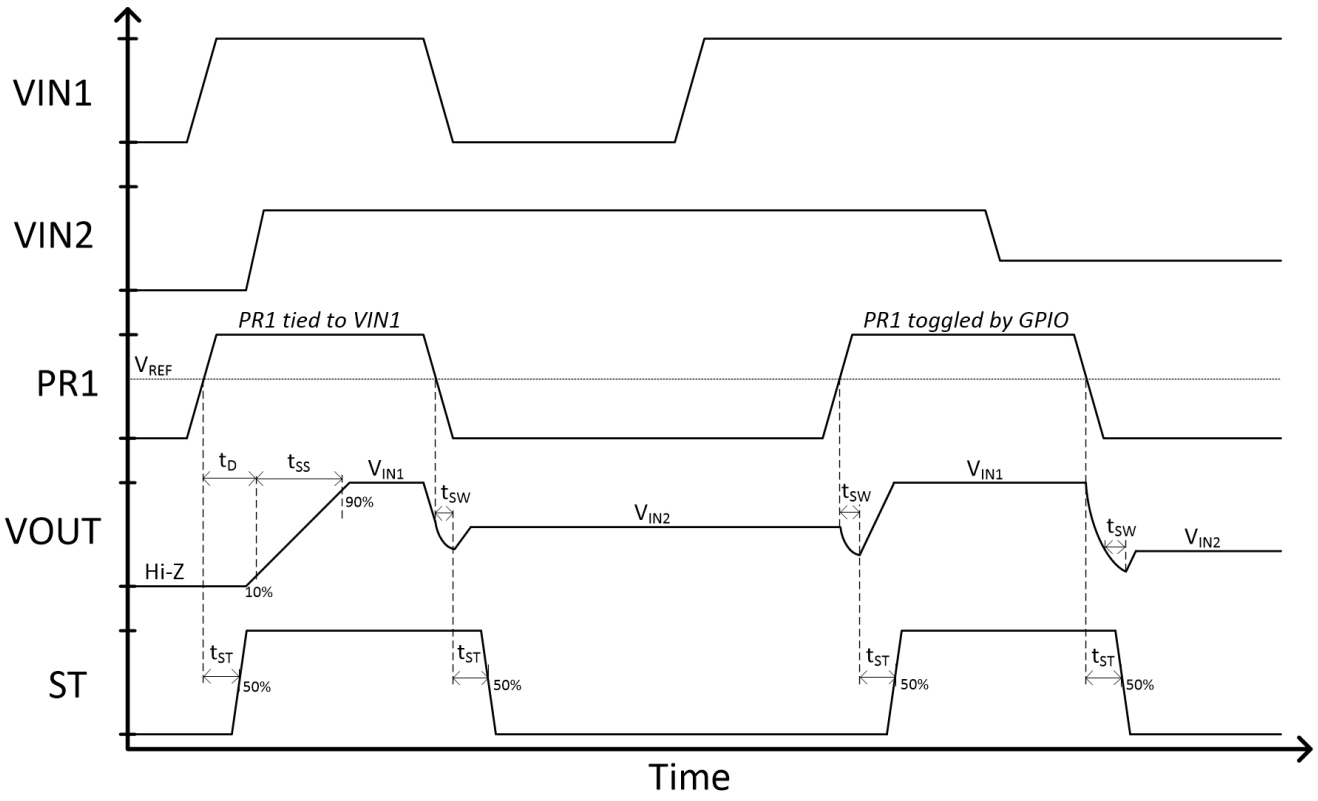


Figure 7-2. Priority/Manual Mode Switching

When PR1 is toggled, the device implements a break-before-make switchover which shuts off both channels before turning on the new channel to power the output. This means that for time t_{SW}, the output is unpowered and will dip depending on the load current and output capacitance. If the output voltage is greater than the input supply being switched to, then the device will not turn on the new channel until the output has discharged down to V_{IN} + V_{RCB} to prevent reverse current flow.

When MODE is pulled low and PR1 is pulled high, the device enters shutdown. Both channels are turned off and the output is high impedance. When the PR1 pin is pulled low, the higher voltage supply between VIN1 and VIN2 is passed to the output.

7.6.1.1 Priority Switching

In the case where VIN1 takes priority over VIN2, a resistor divider can be used to set the switchover voltage threshold. When VIN1 is first applied, PR1 is brought high and VOUT is powered by that input. As VIN1 begins

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to drop, the voltage on PR1 is lowered until it crosses the V_{REF} threshold. At this point, the device switches over to VIN2.

7.6.1.2 Manual Switching

For applications where a GPIO pin is used to select which input passes to the output, the GPIO pin can be directly connected to the PR1 pin when MODE is tied high (≥1V). When the GPIO is pulled high, VIN1 is used, and when the GPIO pin is pulled low, VIN2 is used.

Manual mode can also disable both channels by pulling the MODE pin low and keeping PR1 high. In this state, the output of the device is high impedance and the leakage on each input is the shutdown current, $I_{SD,VINx}$.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

8.2 Typical Application

This typical application demonstrates how the TPS2116 device can be used to control inrush current for high output capacitances.

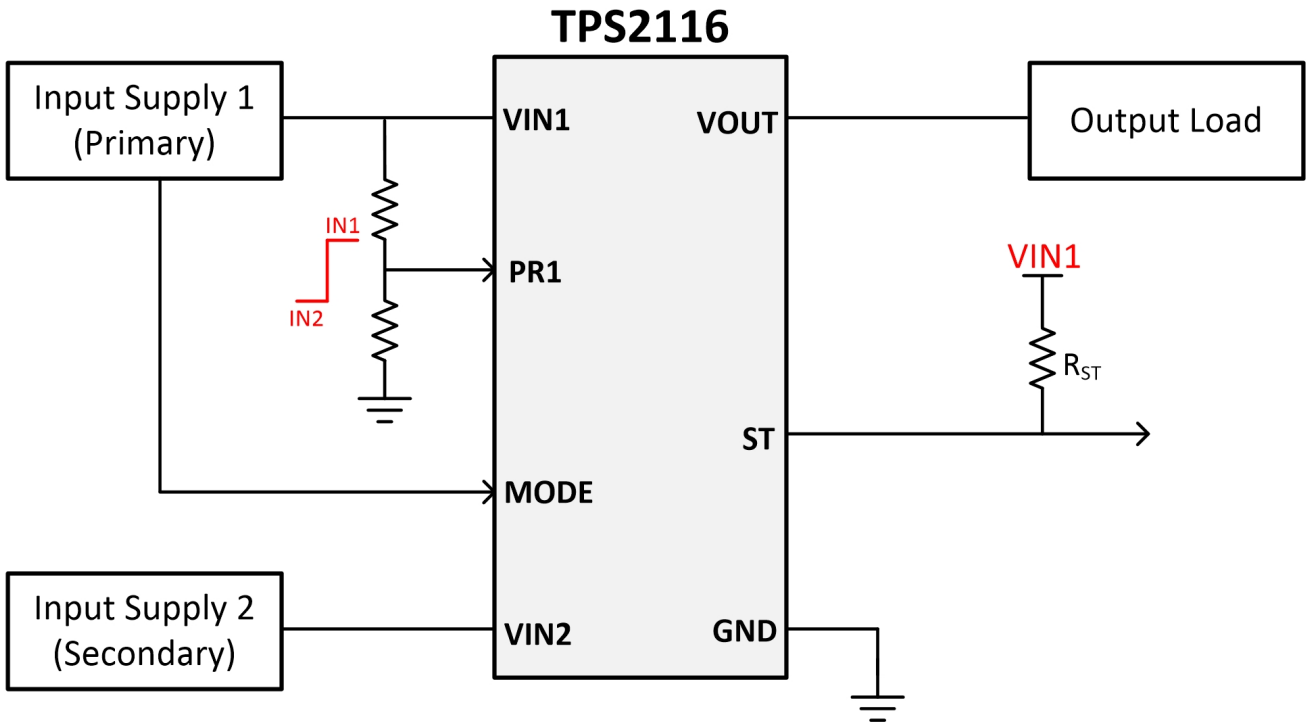


Figure 8-1. TPS2116 Typical Application Diagram

8.2.1 Design Requirements

For this example, the values below are used as the design parameters.

Table 8-1. Design Parameters

PARAMETER	VALUE
VIN1 Input Voltage	5 V
Mode	Priority
Output Capacitance	100 µF
Maximum Inrush Current	500 mA

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8.2.2 Detailed Design Procedure

To determine how much inrush current is caused by the output capacitor, use the equation below.

$$I_{INRUSH} = C_{OUT} \times V_{OUT} / t_{SS} \quad (1)$$

where

- I_{INRUSH} = amount of inrush current caused by C_{OUT}
- C_{OUT} = capacitance on VOUT
- t_{SS} = output voltage soft start time
- V_{OUT} = final value of the output voltage

With a final output voltage of 5 V, the expected rise time is 1.7 ms. Using the inrush current equation, the inrush current caused by a 100-µF capacitance would be 294 mA, well below the 500-mA target.

8.2.3 Application Curves

The below oscilloscope capture shows 5 V being applied to VIN1. The output comes up with slew rate control and limits the inrush current to below 500 mA.

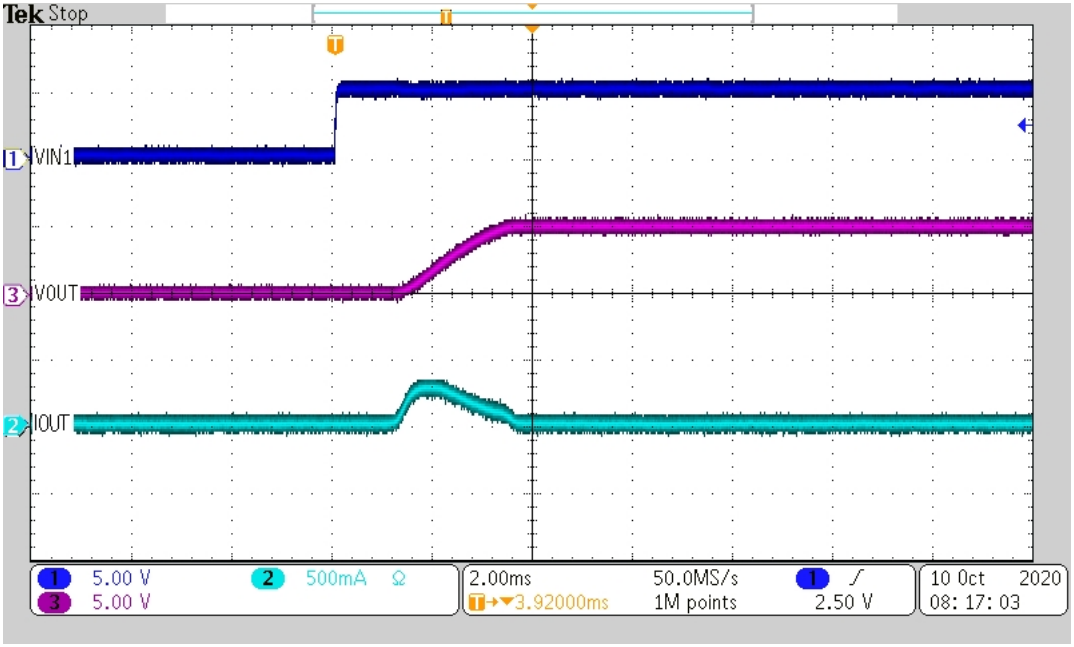


Figure 8-2. TPS2116 Inrush Current Control

9 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supplies must be well regulated and placed as close to the device terminals as possible. The power supplies must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

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10 Layout

10.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN1, VIN2, VOUT, and GND helps minimize the parasitic electrical effects.

10.2 Layout Example

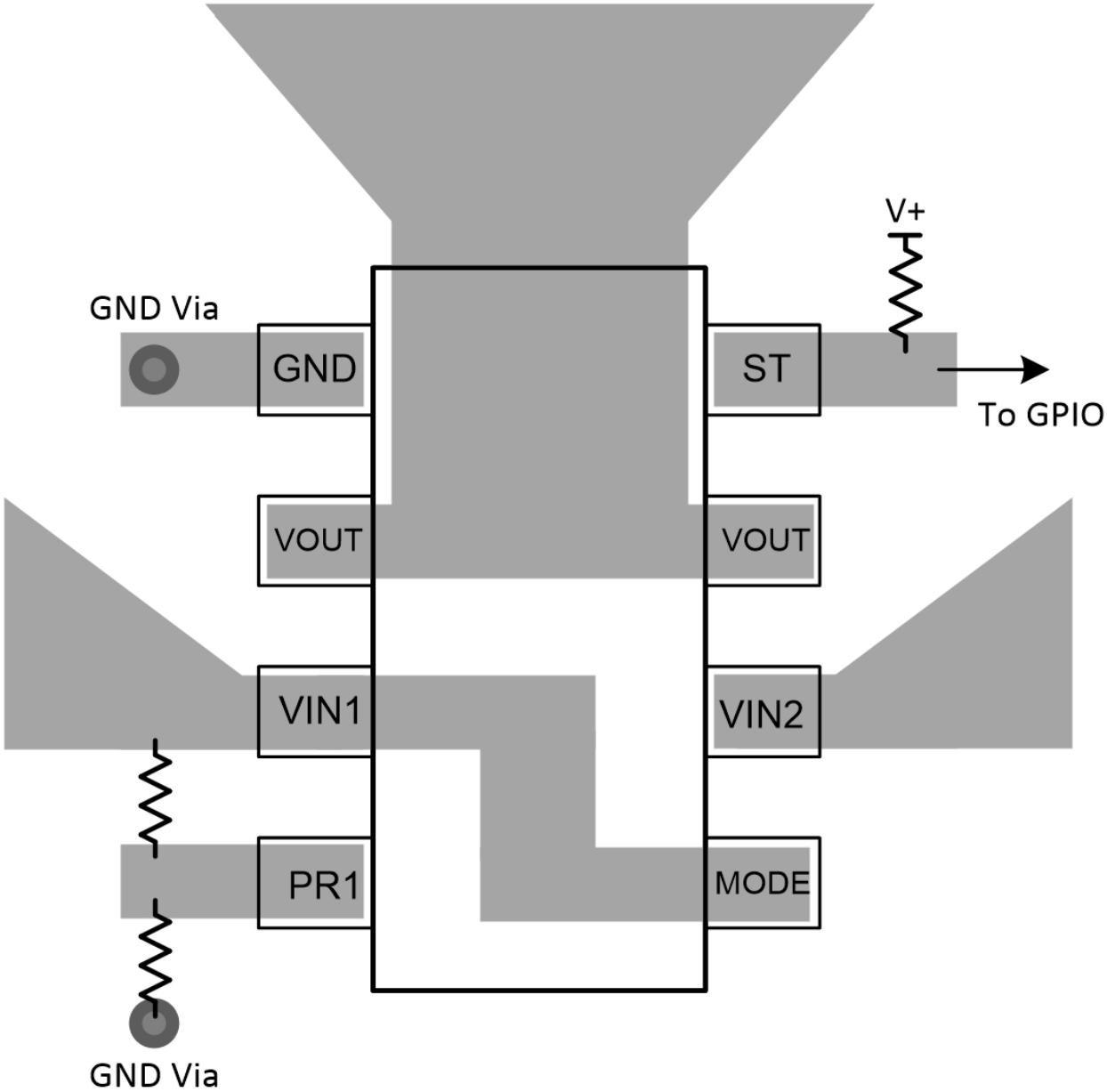


Figure 10-1. TPS2116 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Basics of Power MUX
- 11 Ways to Protect Your Power Path

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2116DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	2116
TPS2116DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2116

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

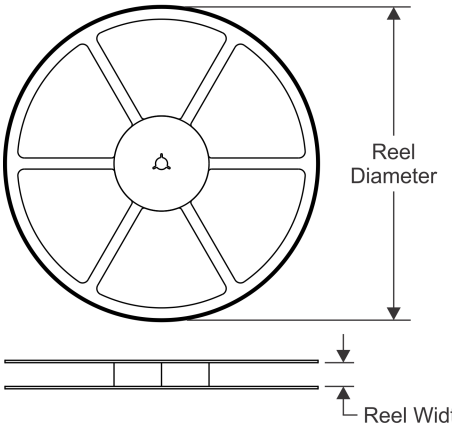
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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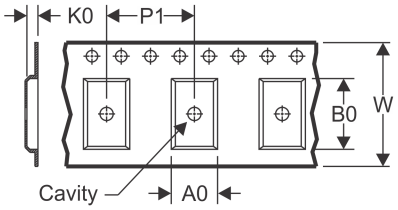
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

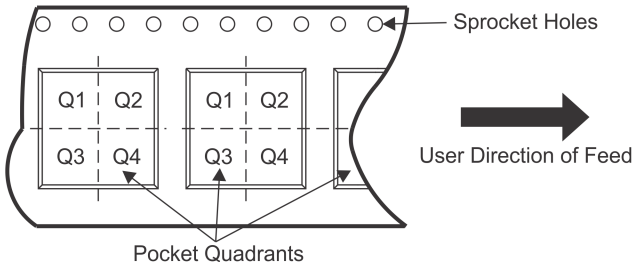


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

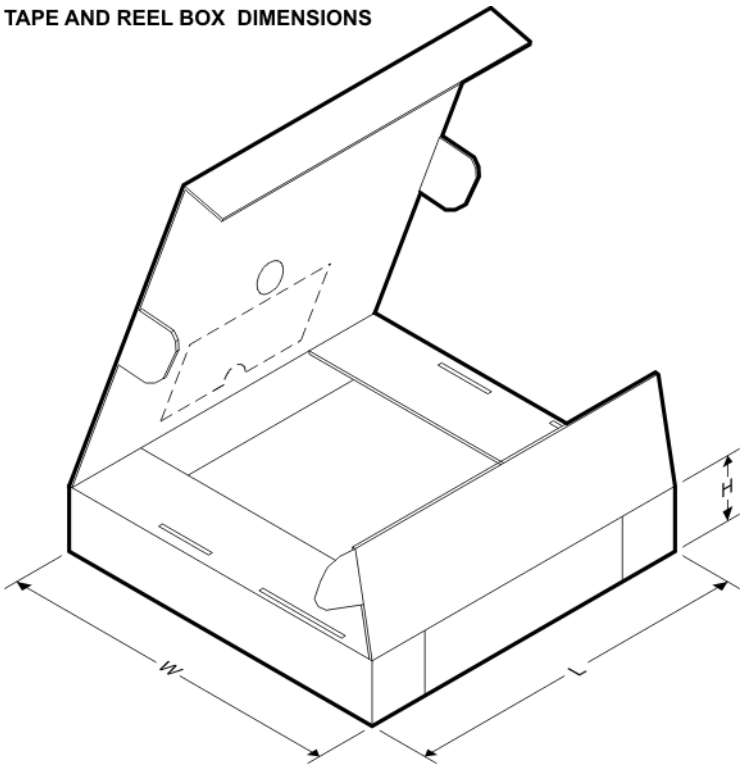
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2116DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2116DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

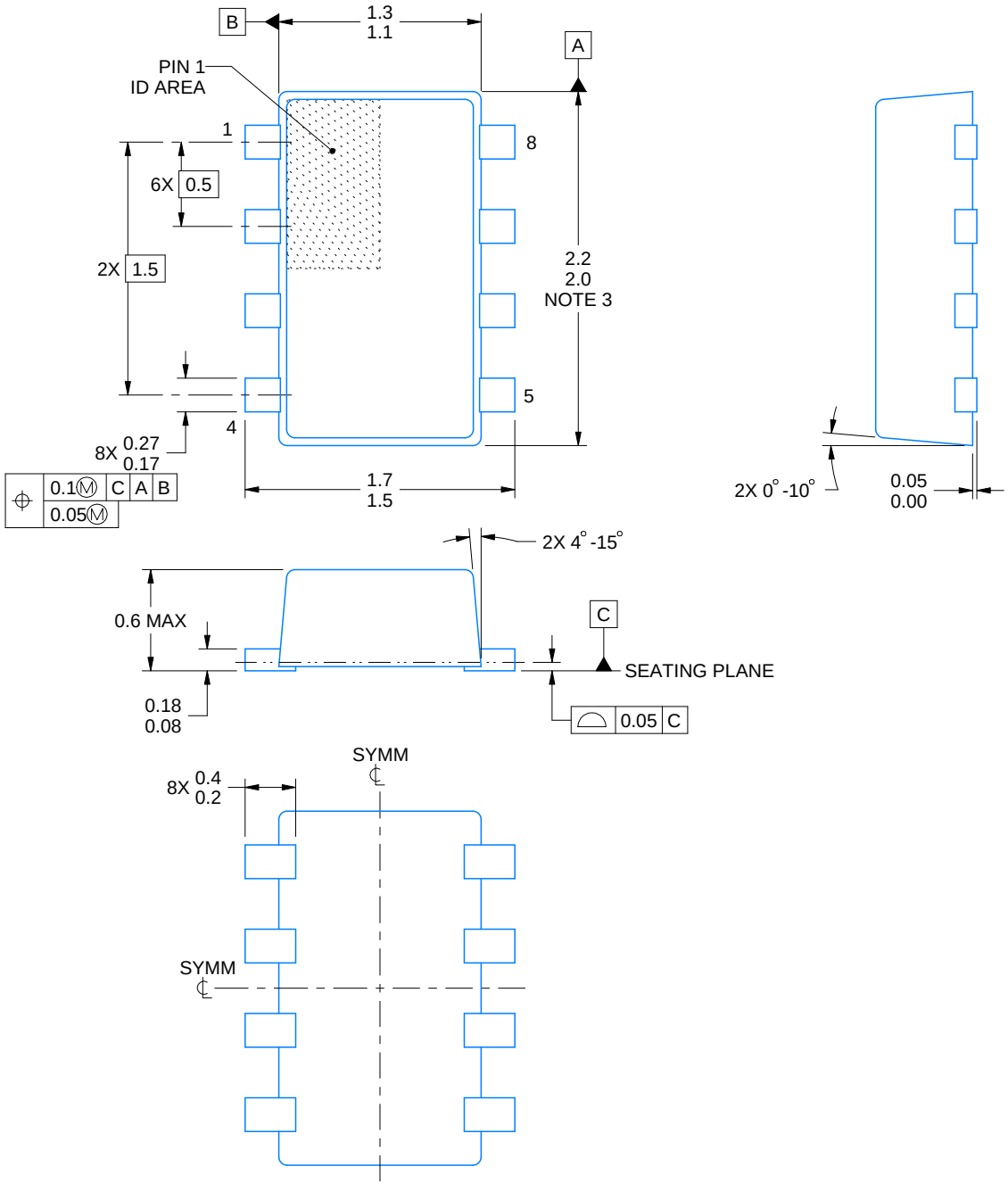


PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

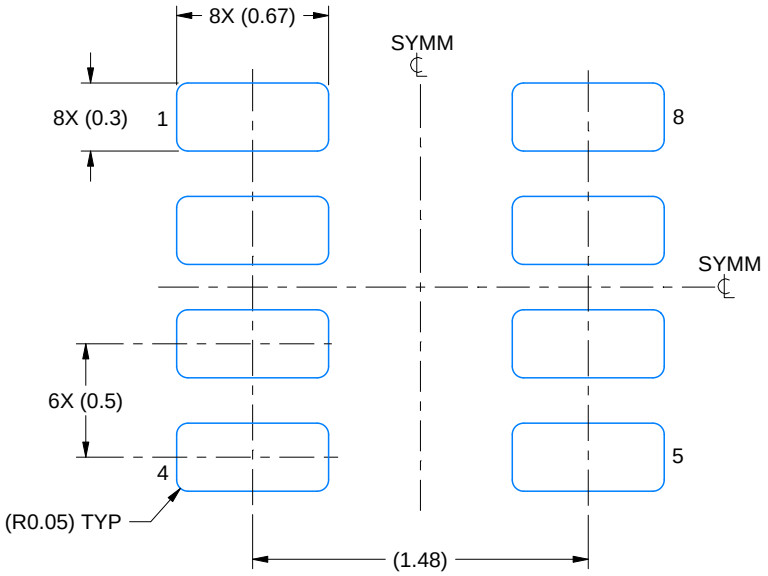
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

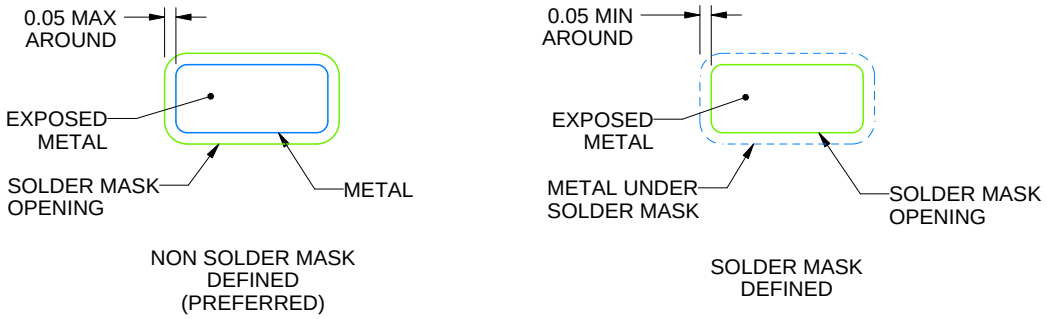
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

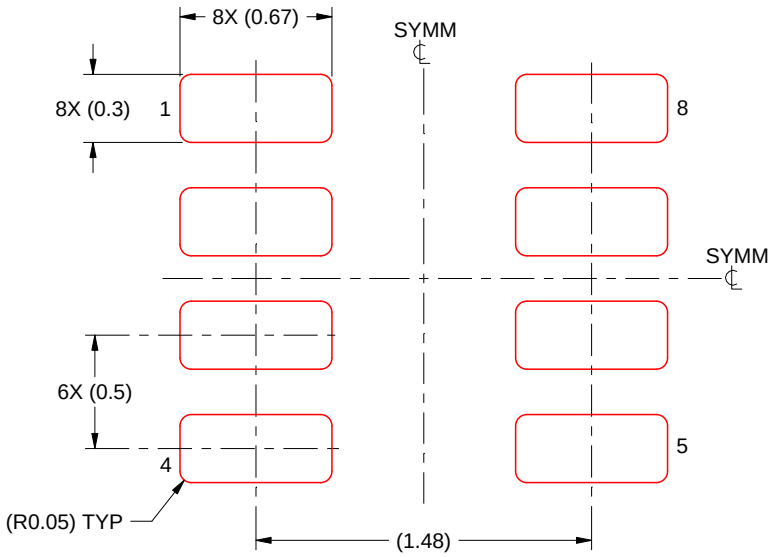
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025

ULN2803C Darlington Transistor Array

1 Features

- 500mA-rated collector current (single output)
- High-voltage outputs: 50V
- Output clamp diodes
- Inputs compatible with various types of logic

2 Applications

- Factory automation and control
- Building automation
- Appliances
- IP network camera
- HVAC valve and actuator control
- Relay, solenoid, and lamp driving
- Stepper motor driving

3 Description

The ULN2803C device is a 50V, 500mA Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500mA. The Darlington pairscan be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803C device has a 2.7kΩ series base resistor for each Darlington pair for operation directly with TTL or 5V CMOS devices.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ULN2803CDW	DW (SOIC, 20)	12.80mm × 10.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Logic Diagram

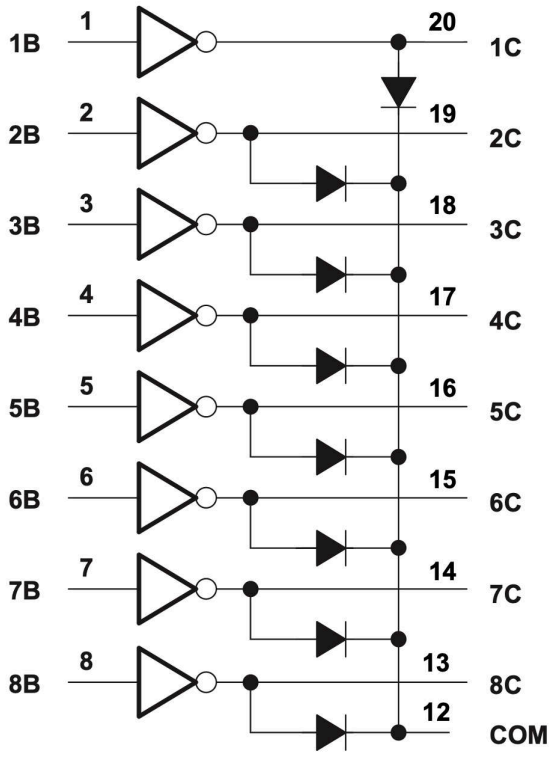


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4 Pin Configuration and Functions

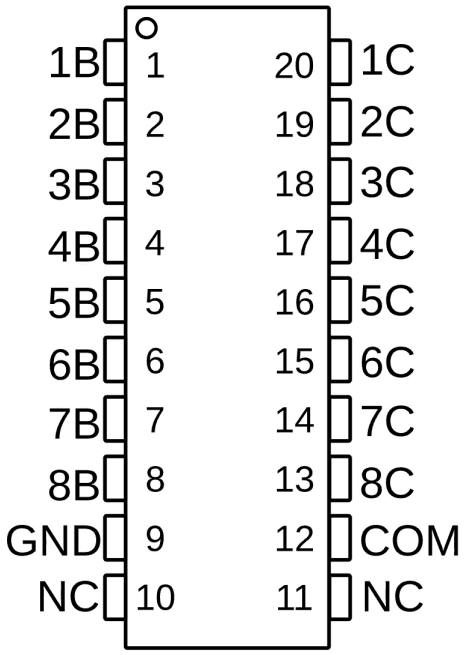


Figure 4-1. DW Package, 20-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 8 Darlington base input.
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
8B	8		
1C	20	O	Channel 1 through 8 Darlington collector output.
2C	19		
3C	18		
4C	17		
5C	16		
6C	15		
7C	14		
8C	13		
GND	9	—	Common emitter shared by all channels (typically tied to ground).
COM	12	I/O	Common cathode node for flyback diodes (required for inductive loads).
NC	10, 11	—	No connect pin.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Collector-emitter voltge		50	V
V_I	Input voltage		30	V
I_C	Peak collector current		500	mA
I_{OK}	Output clamp current		500	mA
I_{MAX}	Total substrate-terminal current		-2.5	A
T_J	Junction temperature	-65	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CE}	Collector-emitter voltge	0		50	V
T_J	Junction temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		ULN2803C DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Typical Values are at 25°C

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Datasheet Specs						

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5.5 Electrical Characteristics (continued)

Typical Values are at 25°C

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$V_{I(ON)}$	ON-state input voltage	V_{CE} = 2V, I_C = 200mA	25°C			2.4	V
		V_{CE} = 2V, I_C = 250mA	25°C			2.7	V
		V_{CE} = 2V, I_C = 300mA	25°C			3	V
$V_{CE(SAT)}$	Colllector-emmiter saturation voltage	I_I = 250uA, I_C = 100mA	25°C		0.9	1.1	V
		I_I = 350uA, I_C = 200mA	25°C		1	1.3	V
		I_I = 500uA, I_C = 350mA	25°C		1.2	1.6	V
I_{CEX}	Collector cutoff current	V_{CE} = 50V, I_I = 0A	25°C			50	uA
V_F	Clamp forward voltage	I_F = 350mA	25°C		1.3	2	V
$I_{I(OFF)}$	OFF-state input current	V_{CE} = 50V, IC = 500uA	70°C	50	65		uA
I_I	Input current	V_I = 3.85V	25°C		0.93	1.35	mA
I_R	Clamp reverse current	V_R = 50V	25°C			50	uA
C_I	Input capacitance	V_I = 0V, f = 1MHz	25°C		15	25	pF

5.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω		130		ns
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω		20		ns
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA	V_S - 20			mV

5.7 Typical Characteristics

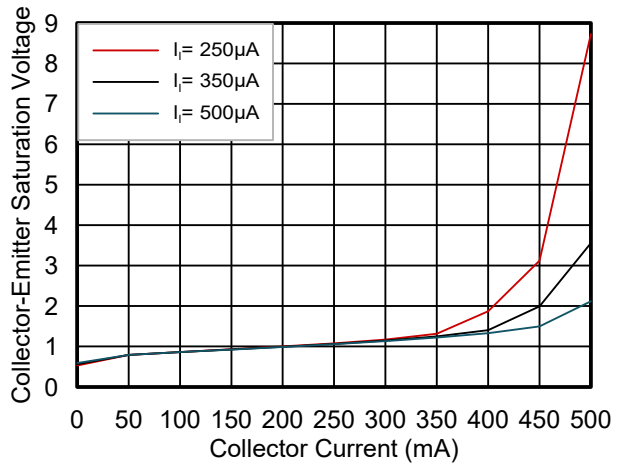


Figure 5-1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

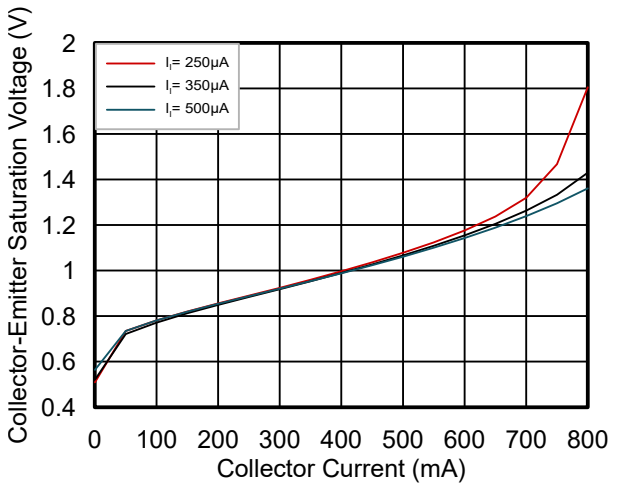


Figure 5-2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

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6 Parameter Measurement Information

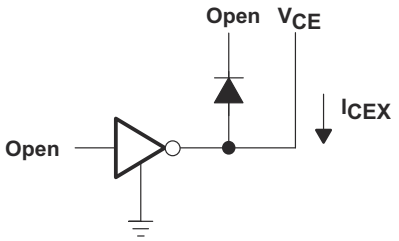


Figure 6-1. I_{CEX} Test Circuit

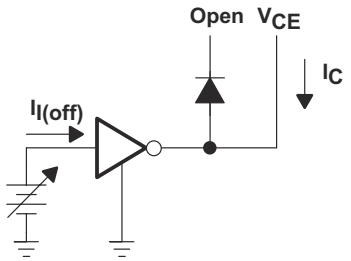


Figure 6-2. $I_{I(off)}$ Test Circuit

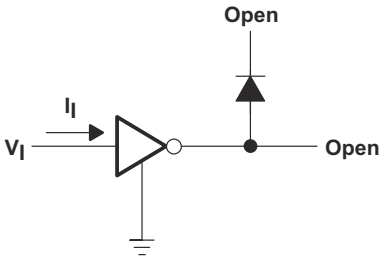


Figure 6-3. $I_{I(on)}$ Test Circuit

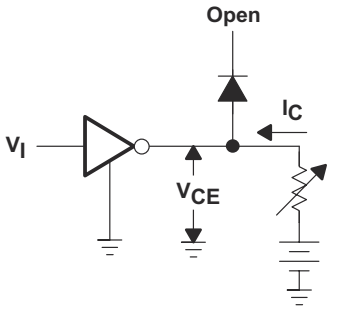


Figure 6-4. $V_{I(on)}$ Test Circuit

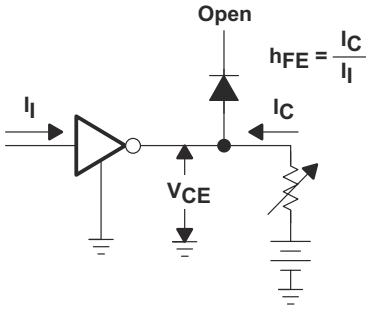


Figure 6-5. h_{FE}, $V_{CE(sat)}$ Test Circuit

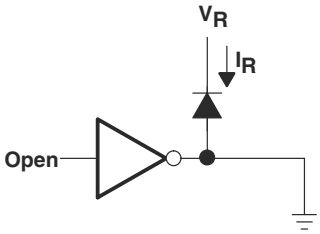


Figure 6-6. I_R Test Circuit

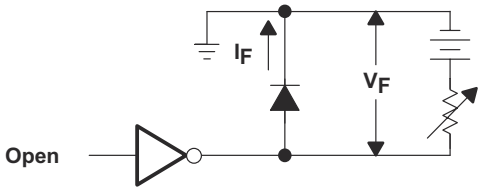
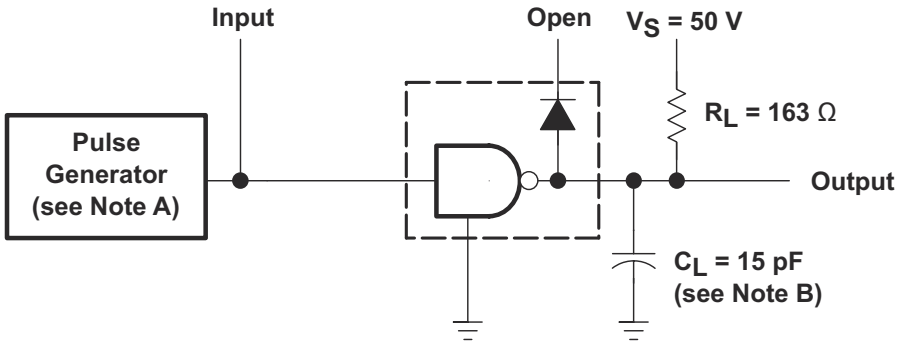
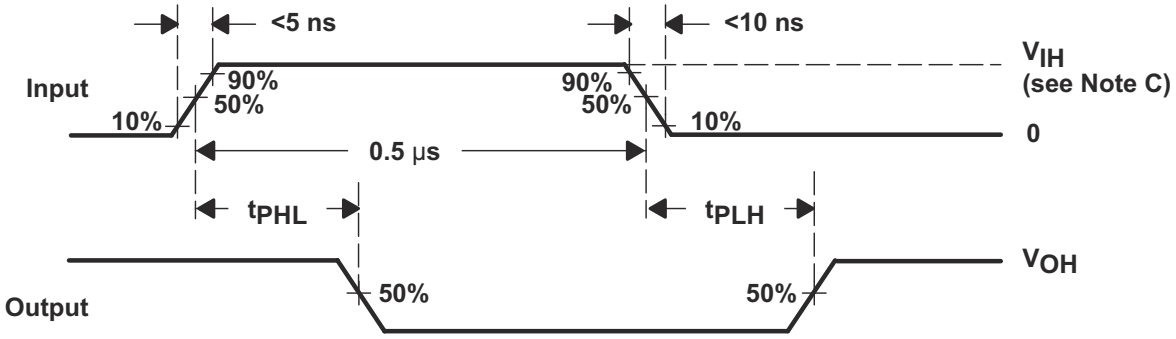


Figure 6-7. V_F Test Circuit

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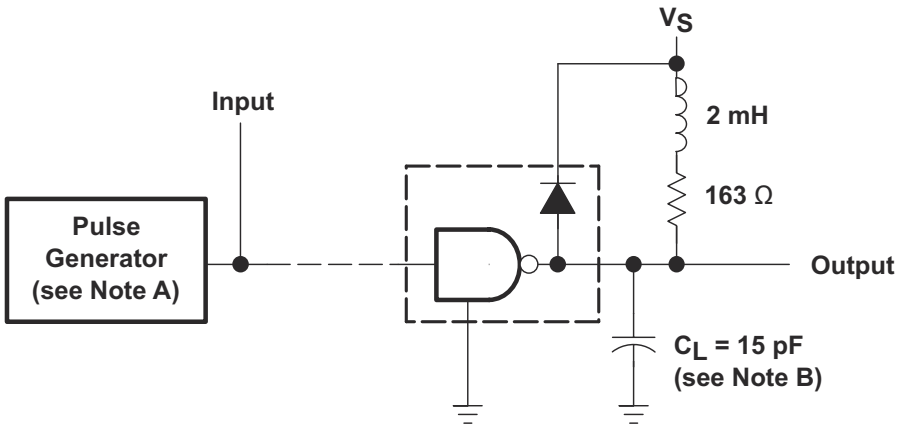
Test Circuit



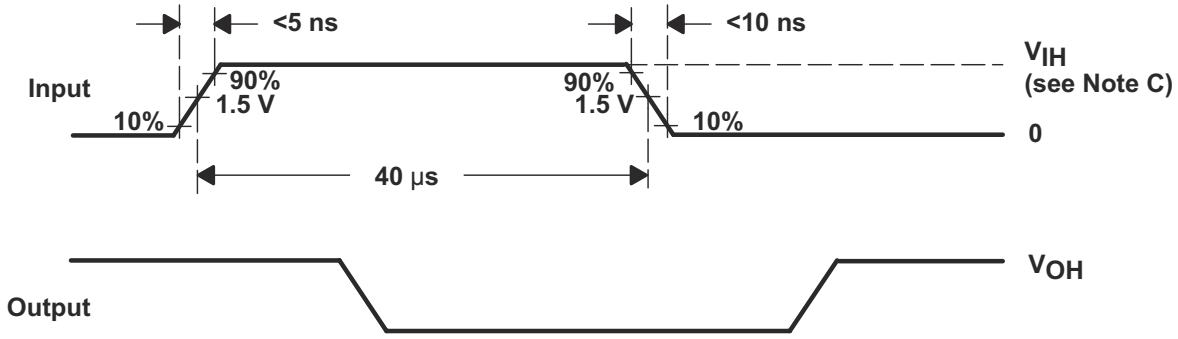
Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 6-8. Propagation Delay Times



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 6-9. Latch-Up Test

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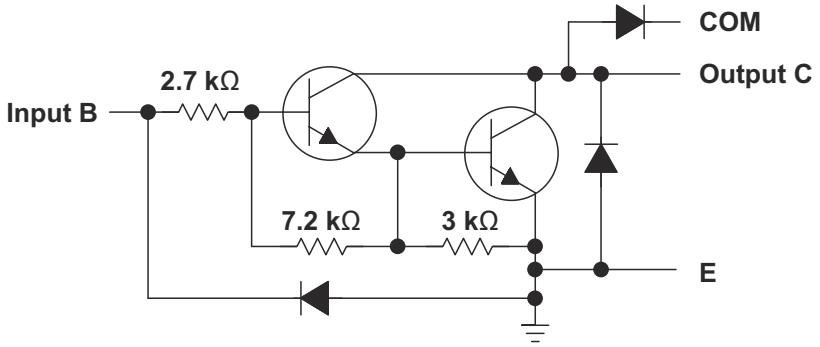
7 Detailed Description

7.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This feature is due to its integration of eight Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803C is comprised of eight high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803C has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2803C offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output can be accommodated by paralleling the outputs.

7.2 Functional Block Diagram



7.3 Feature Description

Each channel of ULN2803C consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very-high current gain. The very high β allows for high output current drive with a very-low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN.

The diodes connected between the output and COM pin are used to suppress the kickback voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kickback diode.

In normal operation, the diodes on base and collector pins to emitter are reverse biased. If these diodes are forward biased, internal parasitic NPN transistors draw (a nearly equal) current from other (nearby) device pins.

7.4 Device Functional Modes

7.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803C can drive inductive loads and suppress the kickback voltage through the internal free wheeling diodes.

7.4.2 Resistive Load Drive

When driving resistive loads, COM can be left unconnected or connected to the load voltage supply. If multiple supplies are used, connect to the highest voltage supply.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

ULN2803C is typically used to drive a high-voltage or current peripherals from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803C, driving inductive loads. This includes motors, solenoids, and relays. Each load type can be modeled by what is seen in Figure 8-1.

8.2 Typical Application

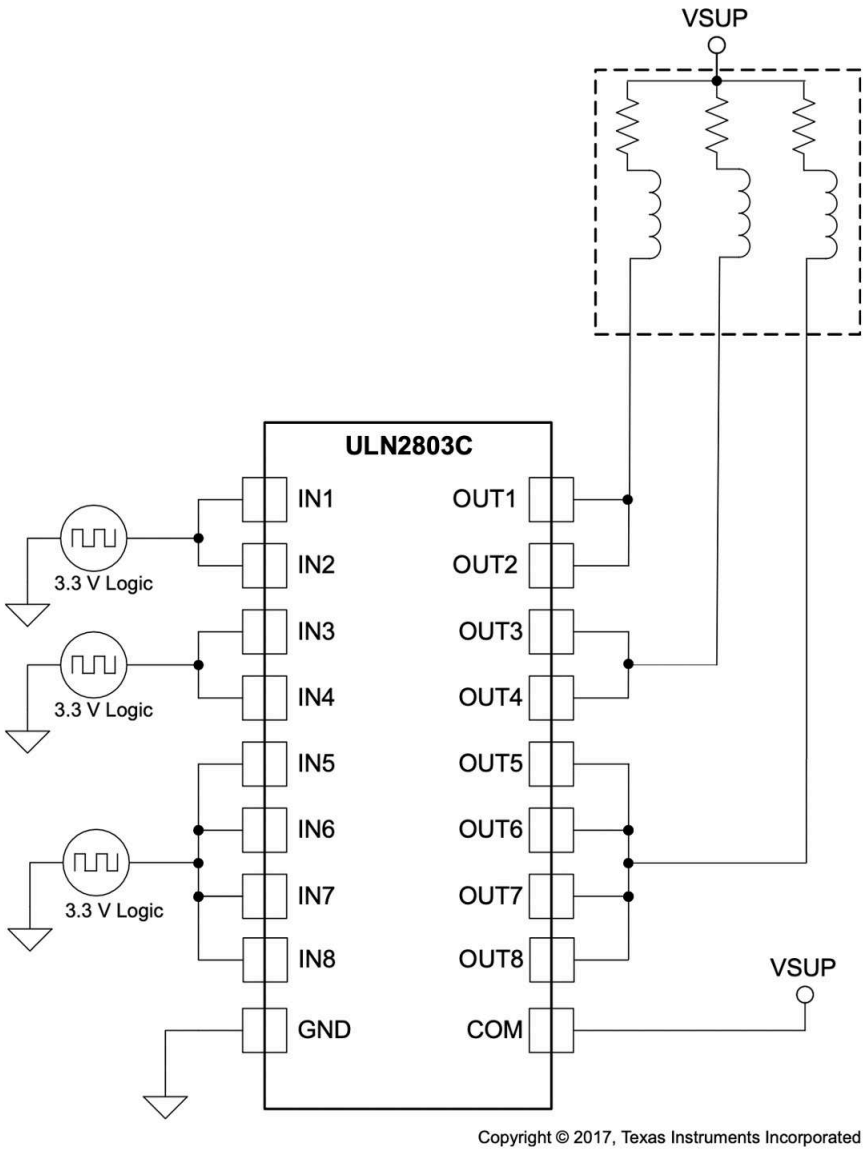


Figure 8-1. ULN2803C as Inductive Load Driver

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8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 or 5 V
Coil supply voltage	12 to 50 V
Number of channels	8
Output current (R_{COIL})	20 to 300 mA per channel
Duty cycle	100%

8.2.2 Detailed Design Procedure

When using ULN2803C in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

8.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance, and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

8.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is equivalent to $V_{CE(SAT)}$ and can be determined by Figure 5-1, Figure 5-2, or using Section 5.5.

8.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use Equation 2 to calculate ULN2803C on-chip power dissipation P_D.

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (2)$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$.

To ensure the reliability of ULN2803C and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (P_D) dictated by Equation 3.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \quad (3)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance.

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TI recommends to limit the ULN2803C IC die junction temperature to < 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

8.2.3 Application Curves

The following curves are generated with ULN2803C driving an OMRON G5NB relay – V_{in} = 5.0 V; V_{sup}= 12 V and R_{COIL}= 2.8 kΩ.

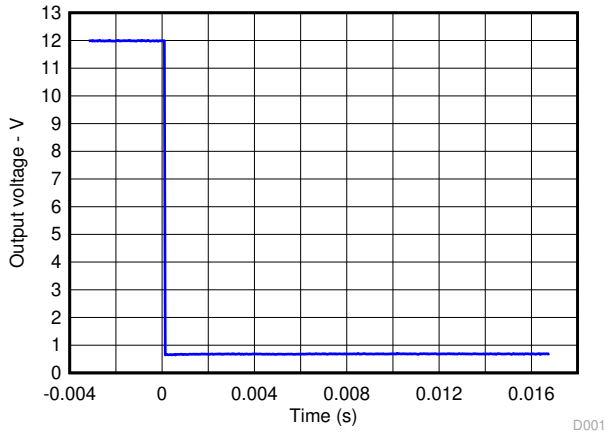


Figure 8-2. Output Response with Activation of Coil (Turn-On)

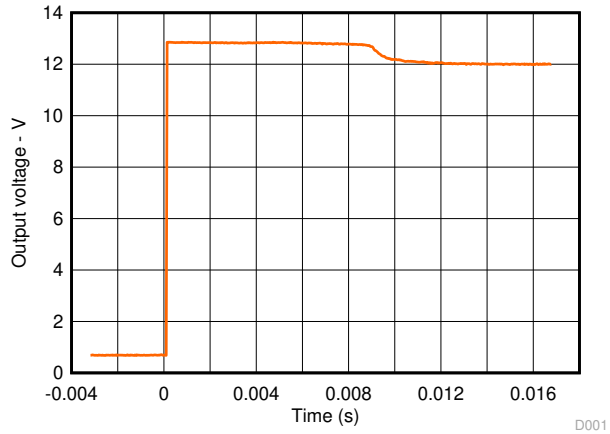


Figure 8-3. Output Response with De-activation of Coil (Turn Off)

8.3 Power Supply Recommendations

This devicedoes not need a power supply; however, the COM pin is typically tied to the system power supply. With this case, make sure that the output voltage does not heavily exceed the COM pin voltage. This action can heavily forward bias the flyback diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or overheating the part.

8.4 Layout

8.4.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803C. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive high currents as desired. Wire thickness can be determined by the trace material current density and desired drive current.

Because all of the channels currents return to a common emitter, size that trace width to be very wide. Some applications require up to 2.5 A.

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8.4.2 Layout Example

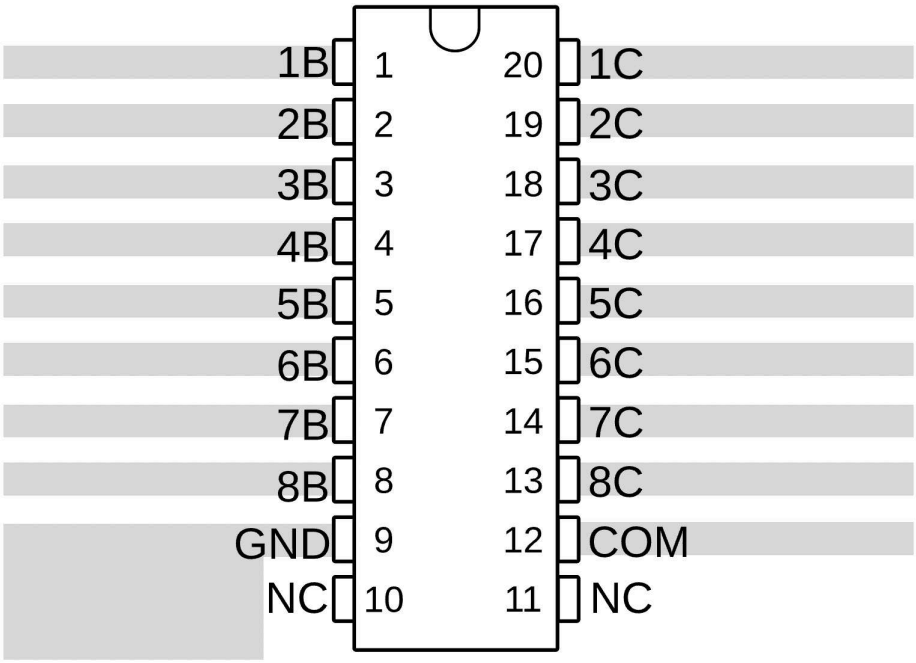


Figure 8-4. ULN2803C Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2024) to Revision B (September 2024)	Page
• Changed part number from ULN2803A to ULN2803C in the *Thermal Information* section	4

Changes from Revision * (August 2022) to Revision A (March 2024)	Page
• Updated thermal parameters in the *Thermal Information* section	4
• Changed typical specification for V_F, Clamp forward voltage from 1.7V : to 1.3V in the *Electrical Characteristics* section	4
• Updated graphs in the *Typical Characteristics* section	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ULN2803CDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULN2803C
ULN2803CDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULN2803C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

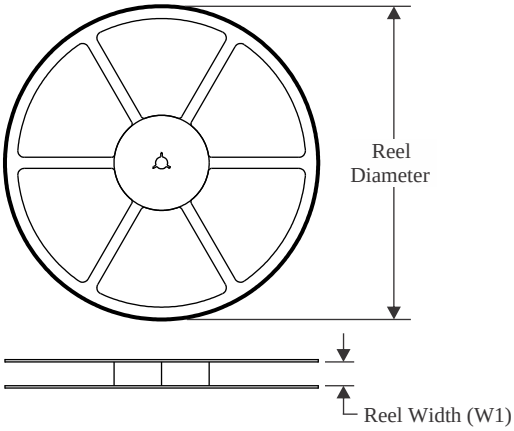
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

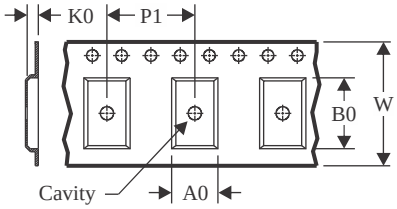
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

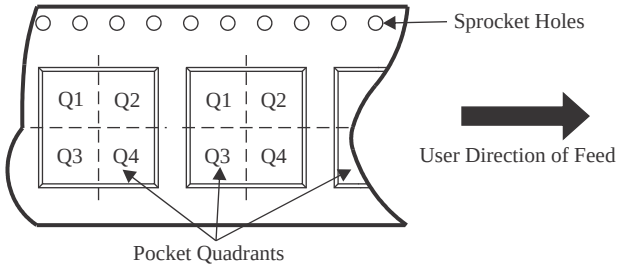


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

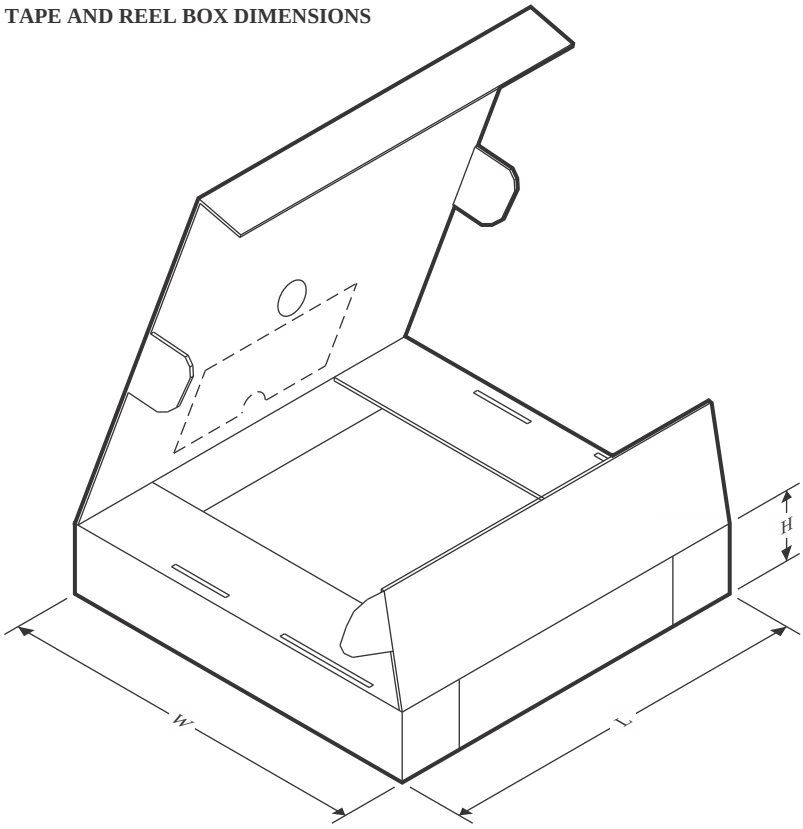
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

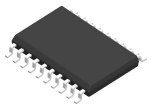
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803CDWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2803CDWR	SOIC	DW	20	2000	356.0	356.0	45.0

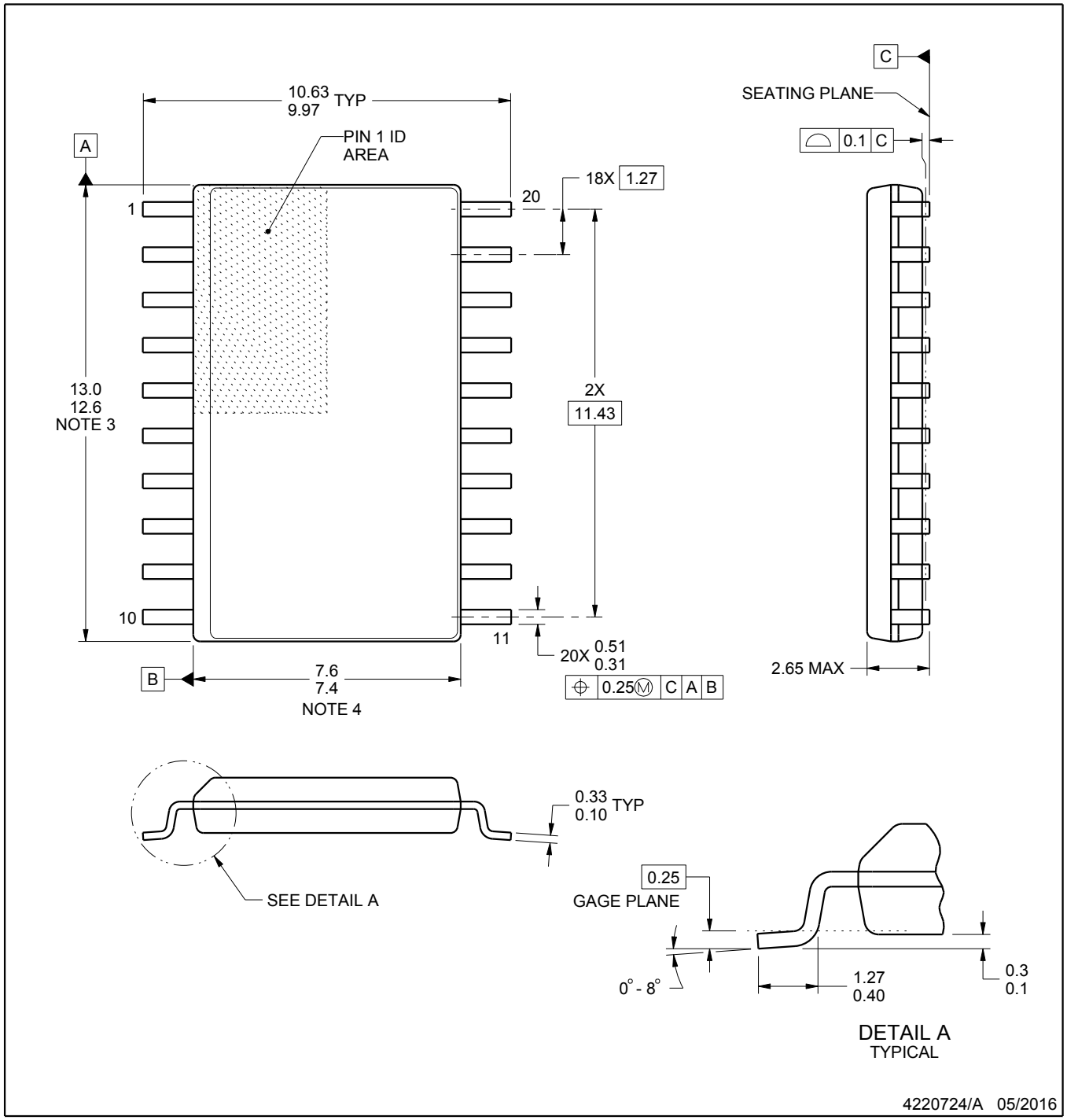


PACKAGE OUTLINE

DW0020A

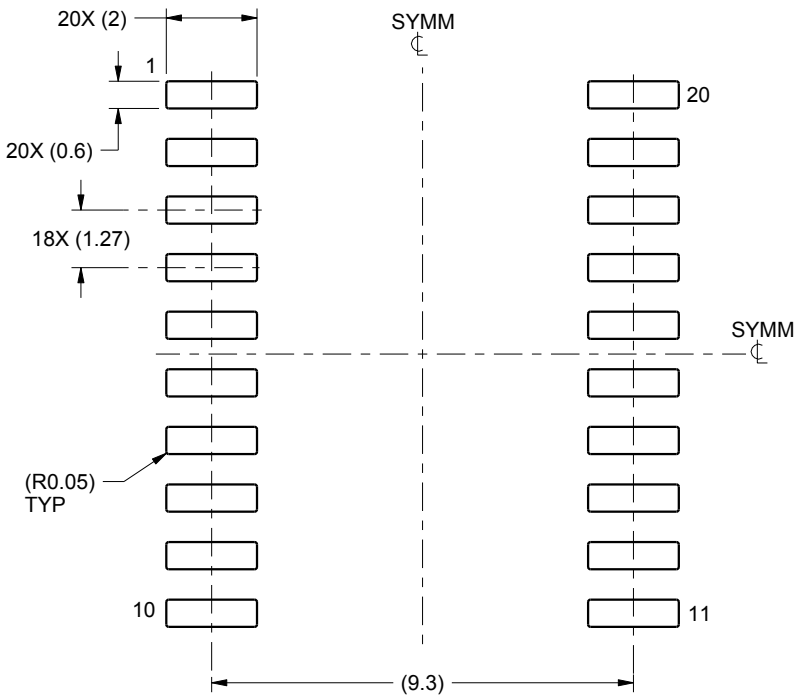
SOIC - 2.65 mm max height

SOIC

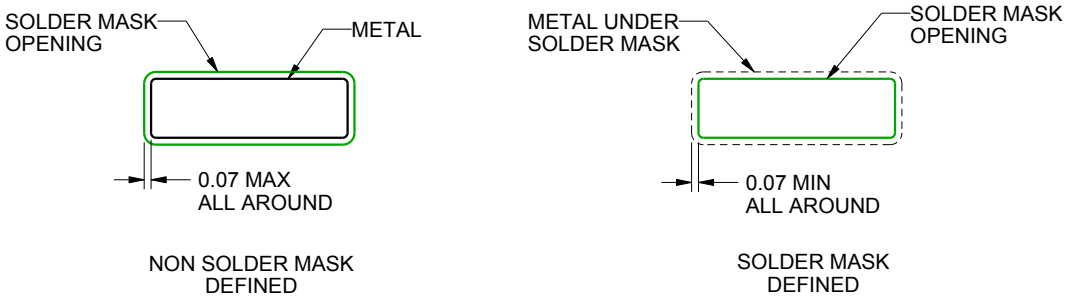


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

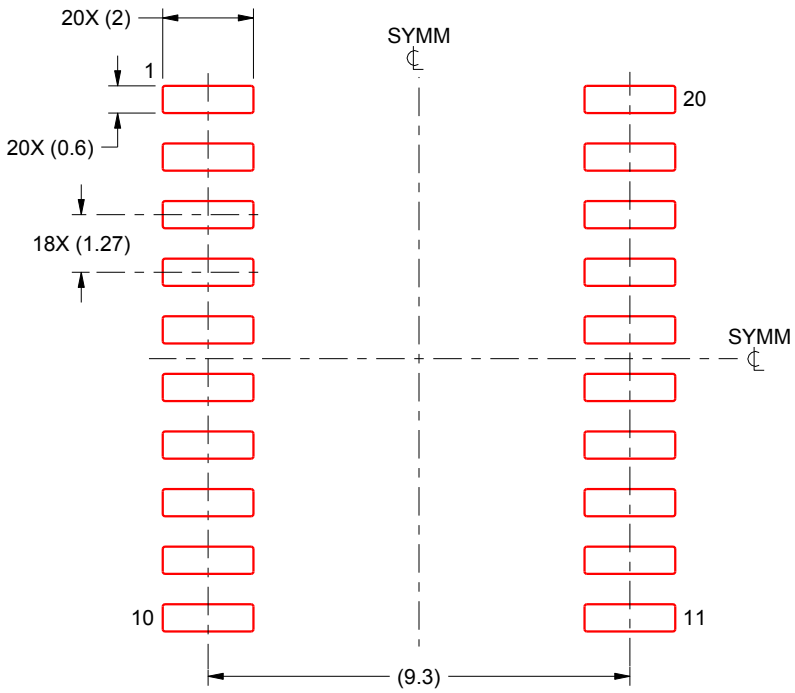


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025

EVVOSEMI®
THINK CHANGE DO

ESD TVS MOS LDO Diode Sensor DC-DC

Product Specification

Domestic Part Number	AMS1117
Overseas Part Number	AMS1117
Equivalent Part Number	AMS1117



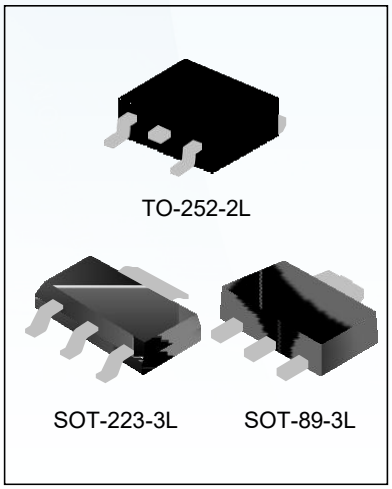
1A LDO Voltage Regulator

DESCRIPTION

The AMS1117 is a positive low voltage dropout regulator; typical voltage dropout is only 1.2V at 1A.

AMS1117 provides two versions: fixed and adjustable versions. VOUT has a tolerance of less than 1.5% for fixed versions 1.2V 1.5V, 1.8V, 2.5V, 3.3V, 5.0V and adjustable version or 2% output accuracy for fixed version 1.2V.

The AMS1117 offers some key features include thermal shutdown and current limiting. It is suitable for all electronic products.



FEATURES

- 1.5% output accuracy for fixed versions 1.2V,1.5V, 1.8V 2.5V, 3.3V, 5.0V and adjustable version
- Adjustable output voltage
- Low Dropout Voltage: Typical 1.2V@1A
- Current Limiting
- Thermal Shutdown
- Temperature Range: -40°C to 125°C

APPLICATIONS

- Laptop, Palmtop, and Notebook Computers
- Battery Charger
- SCSI-II Active Terminator
- Cellular Phone
- Cordless Telephones
- Battery Powered Systems
- Portable Instrumentation
- SMPS Post-Regulator

NOMENCLATURE

AMS1117 □ – □ □

Device

Package
: SOT-223-3L
CD: TO-252-2L
: SOT-89-3L

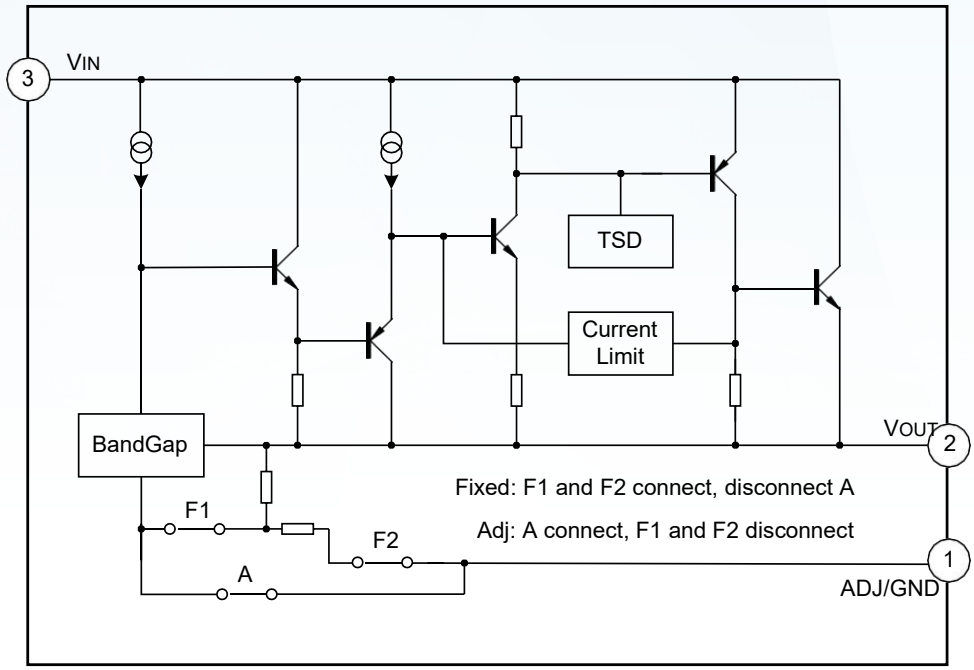
S:SOT-89-3L

ADJ: Adjustable output
1.2: Fixed output 1.2V
1.5: Fixed output 1.5V
1.8: Fixed output 1.8V
2.5: Fixed output 2.5V
3.3: Fixed output 3.3V
5.0: Fixed output 5.0V

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BLOCK DIAGRAM

1A LDO Voltage Regulator



ABSOLUTE MAXIMUM RATINGS

Characteristics		Symbol	Rating	Unit
Input Supply Voltage		V_{IN}	18	V
Lead Temperature (Soldering, 5 seconds)		T_{Lead}	260	°C
Operating Junction Temperature Range		T_J	150	°C
Storage Temperature Range		T_{stg}	-65 ~ +150	V
Power Dissipation		P_D	Internally Limited (Note1)	mW
Thermal Resistance from Junction to Ambient	SOT-223-3L	Rja	88	℃/W
	TO-252-2L		86	
	SOT-89-3L		102	
ESD Tolerance (Minimum)		ESD	2000	V

Note1: The maximum allowable power dissipation is a function of maximum operating junction temperature, T_J (max), the junction to ambient thermal resistance, Rja, and the ambient temperature T_{amb}. The maximum allowable power dissipation at any ambient temperature is given: $P_{D\,(max)} = (T_{J\,(max)} - T_{amb})/ Rja$, exceeding the maximum allowable power limit will result in excessive die temperature; thus, the regulator will go into thermal shutdown. The junction to ambient thermal resistance, θ_{JA} of some packages may be different, The value of θ_{JA} depends on mounting technique.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Rating	Unit
Input voltage	V_{IN}	12	V
Operating Junction Temperature Range	T_J	-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

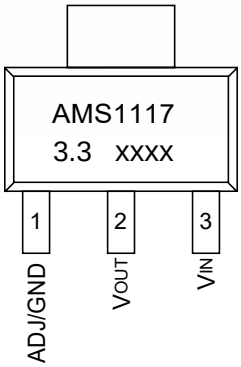
Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference Voltage	V_{REF}	AMS1117-ADJ, I_{OUT}=10mA, V_{IN}-V_{OUT}=2V, T_J=25°C 10mA≤I_{OUT}≤1A, 1.4V≤V_{IN}-V_{OUT}≤10V	1.231 1.225	1.250 1.250	1.268 1.275	V
Output Voltage	V_{OUT}	AMS1117-1.2, I_{OUT}=10mA, V_{IN}=3.2V ,T_J=25°C 10mA≤I_{OUT}≤1A, 3.0V≤V_{IN}≤10V	1.176 1.152	1.2 1.2	1.224 1.248	V
		AMS1117-1.5, I_{OUT}=10mA, V_{IN}=3.5V ,T_J=25°C 10mA≤I_{OUT}≤1A, 3.0V≤V_{IN}≤10V	1.477 1.470	1.500 1.500	1.5221 .530	V
		AMS1117-1.8, I_{OUT}=10mA, V_{IN}=3.8V, T_J=25°C , 0≤I_{OUT}≤1A, 3.2V≤V_{IN}≤10V	1.7731 .746	1.800 1.800	1.827 1.854	V
		AMS1117-2.5, I_{OUT}=10mA, V_{IN}=4.5V,T_J=25°C , 0≤I_{OUT}≤1A, 3.9V≤V_{IN} ≤10V	2.462 2.450	2.500 2.500	2.538 2.550	V
		AMS1117-3.3, I_{OUT}=10mA, V_{IN}=5V,T_J=25°C , 0≤I_{OUT}≤1A, 4.75V≤V_{IN}≤10V	3.250 3.235	3.300 3.300	3.349 3.365	V
		AMS1117-5.0, I_{OUT}=10mA, V_{IN}=7V, T_J=25°C , 0≤ I_{OUT}≤1A, 6.5V≤V_{IN}≤12V	4.925 4.900	5.000 5.000	5.075 5.10	V
Output Voltage Temperature Stability	TS_{OUT}		--	0.3	--	%
Line Regulation	R_{line}	V_{INMIN} ≤V_{IN}≤ 12V, V_{OUT}=Fixed/Adj,I_{OUT}=10mA	--	9	18	mV
Load Regulation	R_{load}	10mA≤I_{OUT}≤1A, V_{OUT}=Fixed/Adj	--	10	18	mV
Dropout Voltage	V_{drop}	I_{OUT}=100mA I_{OUT}=500mA I_{OUT}=1A	--	1.00 1.05 1.20	1.20 1.25 1.30	V
Quiescent Current	I_q	4.25V≤V_{IN}≤ 6.5V	--	5	10	mA
Ripple Rejection	P_{SRR}	f_{RIPPLE}=120Hz, (V_{IN}-V_{OUT})=3V, V_{RIPPLE}=1V_{PP}	60	75	--	dB
Adjust pin Current	I_{adj}		--	60	120	μA
Adjust pin Current Change		0≤ I_{OUT}≤1A, 1.4V ≤V_{IN}-V_{OUT}≤10V	--	0.2	5	μA
Thermal shutdown	TSD		--	150	--	°C
Current limitting	I_{limit}		2.1	--	2.5	A
Temperature Stabiliy			--	0.5	--	%
Long Term Stability		T_A=125°C, 1000Hrs	--	0. 3	--	%

1A LDO Voltage Regulator

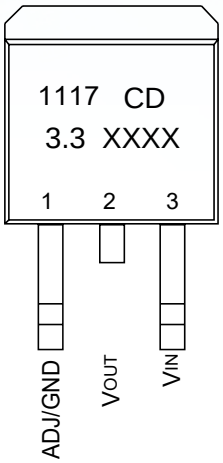
Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
RMS Output Noise		% of V_{OUT}, 10Hz≤f≤10kHz	--	0.003	--	%

PIN CONFIGURATION

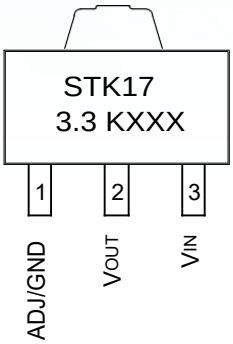
SOT-223-3L



TO-252-2L



SOT-89-3L



PIN DESCRIPTION

Pin No.	Pin name	I/O	Functions
1	GND/ADJ	--/O	Ground/ADJ
2	VOUT	O	Output voltage
3	VIN	I	Input supply voltage

FUNCTION DESCRIPTION

The AMS1117 is a LDO regulator, it's pass transistor is made up of a single NPN transistor being driven by a PNP. The dropout voltage is defined as: $V_{DROP} = V_{BE} + V_{SAT}$.

The AMS1117 series of fixed and adjustable regulators are easy to use. Output voltages are 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5.0V.On-chip thermal shut down provides protection against any combination of overload and ambient temperature that would create excessive junction temperature.

The AMS1117 requires an output capacitor for device stability. Its value of 22μF tantalum covers all cases of bypassing the adjustment terminal. Without bypassing the adjustment terminal smaller capacitors can be used with equally good results which depend upon the application circuit. In general, linear regulator stability decreases with higher output currents.

TYPICAL APPLICATION CIRCUIT

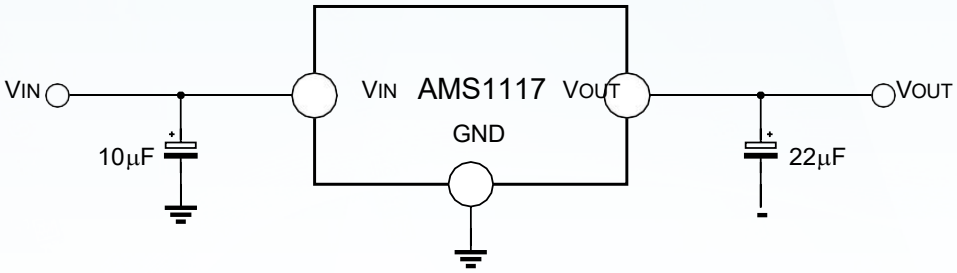


Figure 1. Typical Fixed Output Voltage

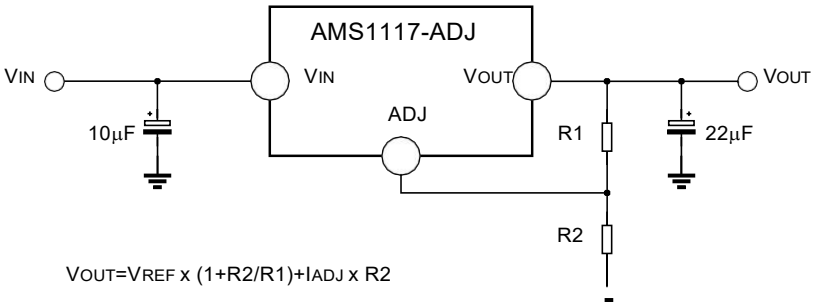
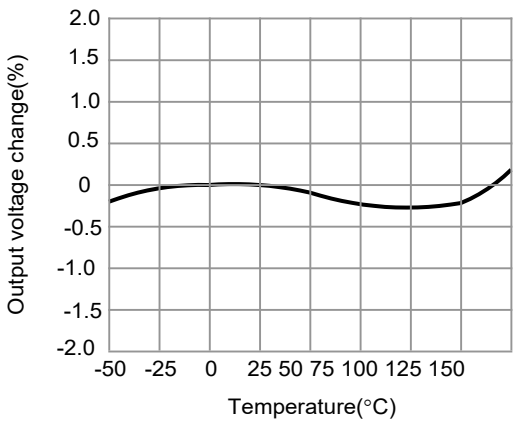


Figure 2. Typical Adjustable Output Voltage

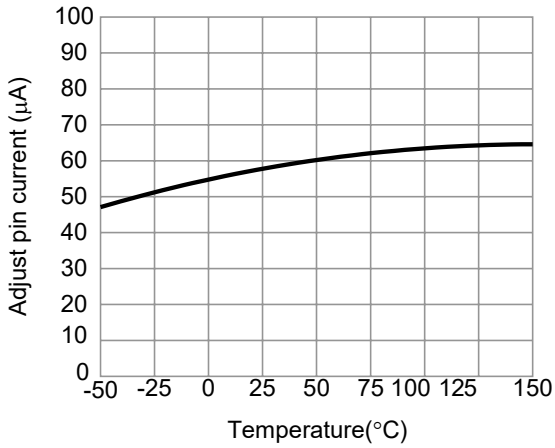
Note: The circuit and parameters are reference only, please set the parameters of the real application circuit based on the real test.

TYPICAL CHARACTERISTICS

Temperature Stability

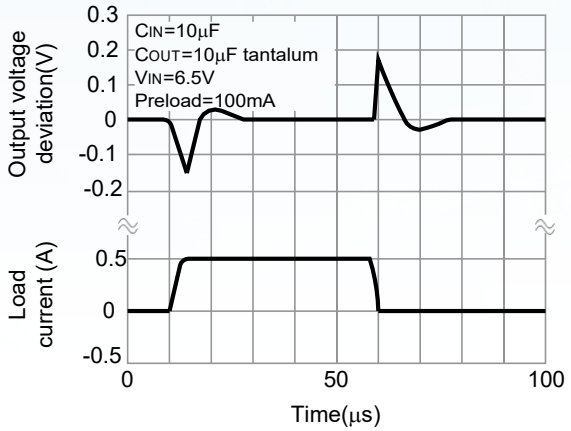


Adjust Pin Current

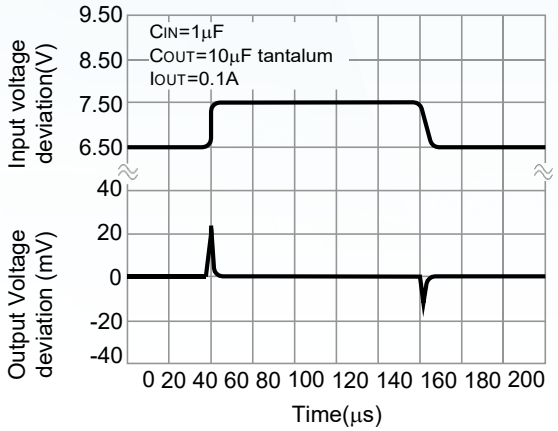


TYPICAL CHARACTERISTICS CURVES(continued)

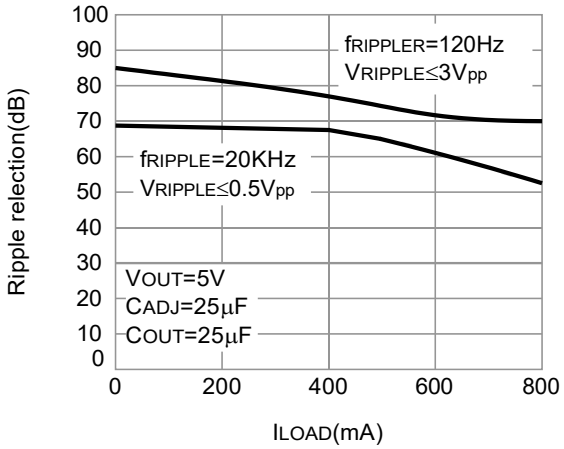
V_{OUT}=5 V Load Transient Response



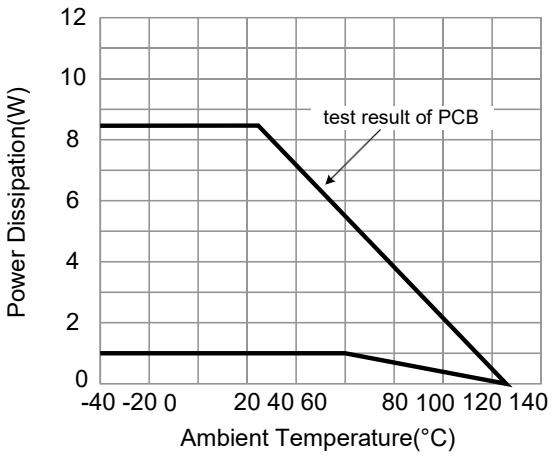
V_{OUT}=5 V Line Transient Response



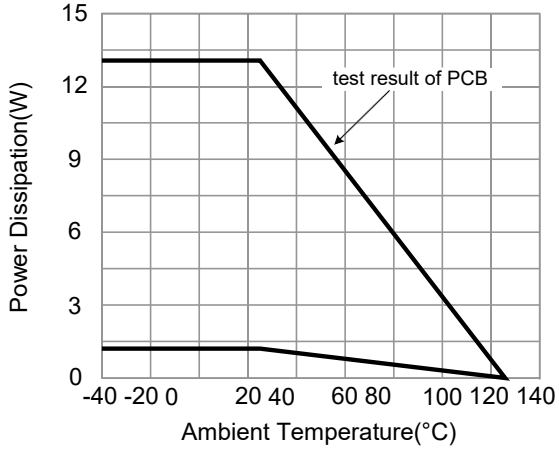
Ripple Rejection VS Current



Power Dissipation VS Ambient Temperature(SOT-223)



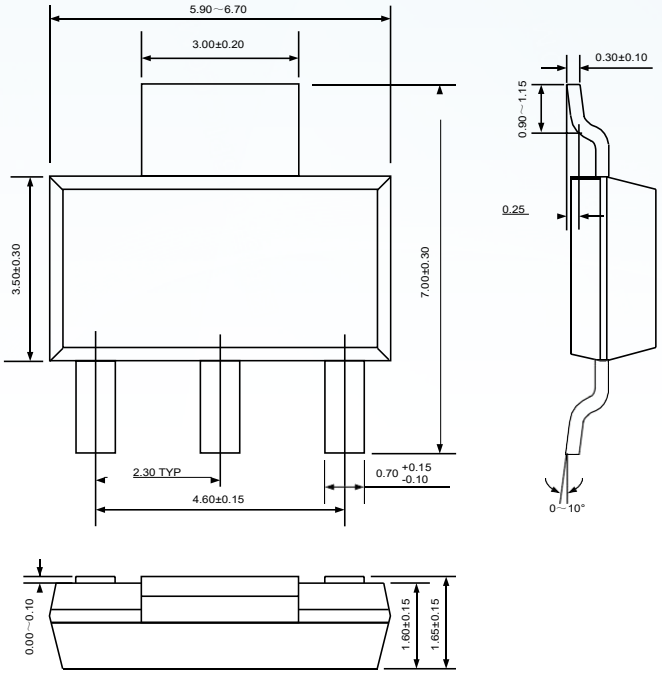
Power Dissipation VS Ambient Temperature(TO-252)



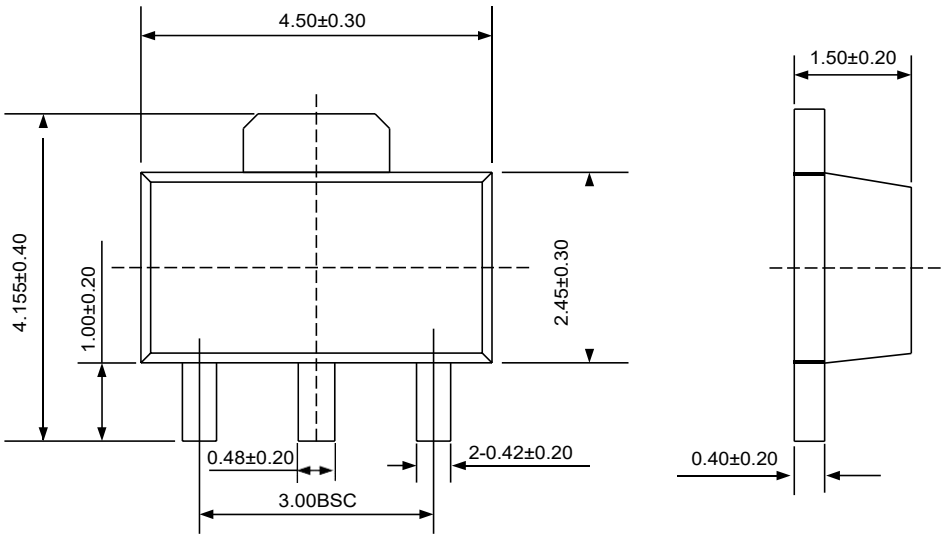
PACKAGE OUTLINE

1A LDO Voltage Regulator

SOT-223-3L UNIT: mm

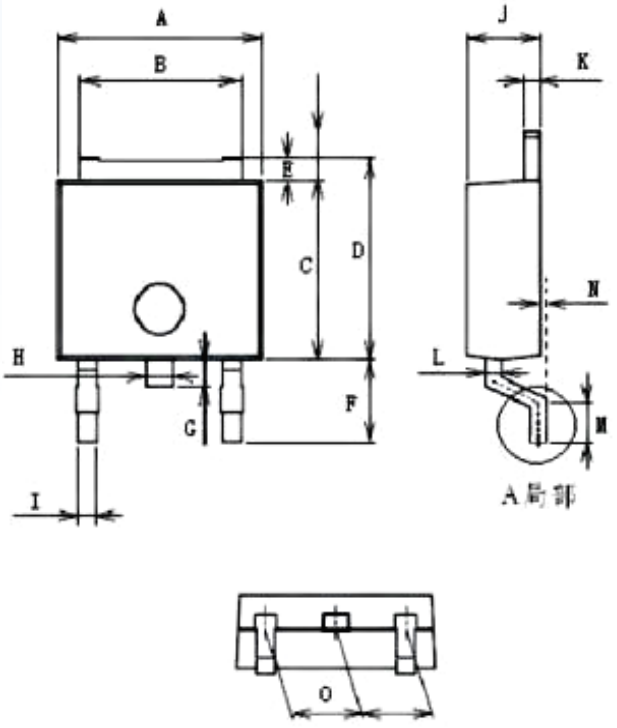


SOT-89-3L UNIT: mm



PACKAGE OUTLINE **(continued)**

TO-252-2L UNIT: mm



Unit: mm

Item	Min	Max
A	6. 40	6. 70
B	5. 20	5. 40
C	6. 00	6. 30
D	6. 55	6. 85
E	0. 45	0. 60
F	3. 07	3. 35
G	0. 85	1. 05
H	0. 75	0. 95
I	0. 55	0. 75
J	2. 20	2. 40
K	0. 43	0. 58
L	0. 43	0. 58
M	0. 90	1. 10
N	0. 90	1. 10
O	2. 20	2. 40

NOTE1: There are two conditions for this position:has an eject pin or has no eject pin.

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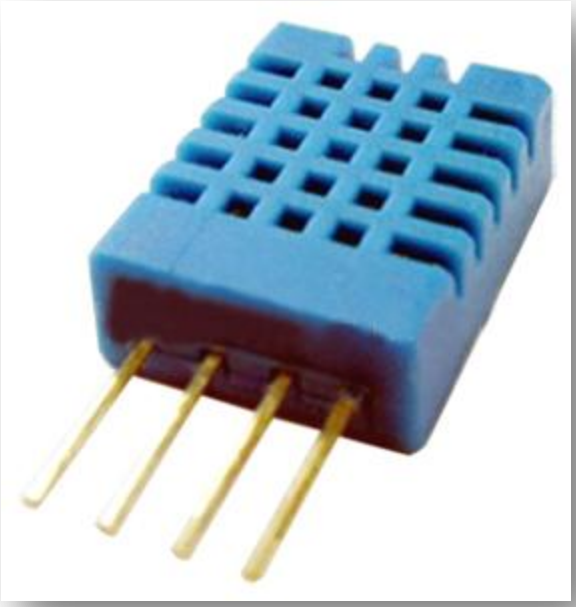
DHT11 Humidity & Temperature Sensor

DHT11 Temperature & Humidity Sensor features a temperature & humidity sensor complex with a calibrated digital signal output.

DHT 11 Humidity & Temperature Sensor

1. Introduction

DHT11 Temperature & Humidity Sensor features a temperature & humidity sensor complex with a calibrated digital signal output. By using the exclusive digital-signal-acquisition technique and temperature & humidity sensing technology, it ensures high reliability and excellent long-term stability. This sensor includes a resistive-type humidity measurement component and an NTC temperature measurement component, and connects to a high-performance 8-bit microcontroller, offering excellent quality, fast response, anti-interference ability and cost-effectiveness.



Each DHT11 element is strictly calibrated in the laboratory that is extremely accurate on humidity calibration. The calibration coefficients are stored as programmes in the OTP memory, which are used by the sensor's internal signal detecting process. The single-wire serial interface makes system integration quick and easy. Its small size, low power consumption and up-to-20 meter signal transmission making it the best choice for various applications, including those most demanding ones. The component is 4-pin single row pin package. It is convenient to connect and special packages can be provided according to users' request.

2. Technical Specifications:

Overview:

Item	Measurement Range	Humidity Accuracy	Temperature Accuracy	Resolution	Package
DHT11	20-90%RH 0-50 ℃	±5%RH	±2℃	1	4 Pin Single Row

Detailed Specifications:

Parameters	Conditions	Minimum	Typical	Maximum
Humidity				
Resolution		1%RH	1%RH	1%RH
			8 Bit	
Repeatability			±1%RH	
Accuracy	25℃		±4%RH	
	0-50℃			±5%RH
Interchangeability	Fully Interchangeable			
Measurement Range	0℃	30%RH		90%RH
	25℃	20%RH		90%RH
	50℃	20%RH		80%RH
Response Time (Seconds)	1/e(63%)25℃, 1m/s Air	6 S	10 S	15 S
Hysteresis			±1%RH	
Long-Term Stability	Typical		±1%RH/year	
Temperature				
Resolution		1℃	1℃	1℃
		8 Bit	8 Bit	8 Bit
Repeatability			±1℃	
Accuracy		±1℃		±2℃
Measurement Range		0℃		50℃
Response Time (Seconds)	1/e(63%)	6 S		30 S

3. Typical Application (Figure 1)

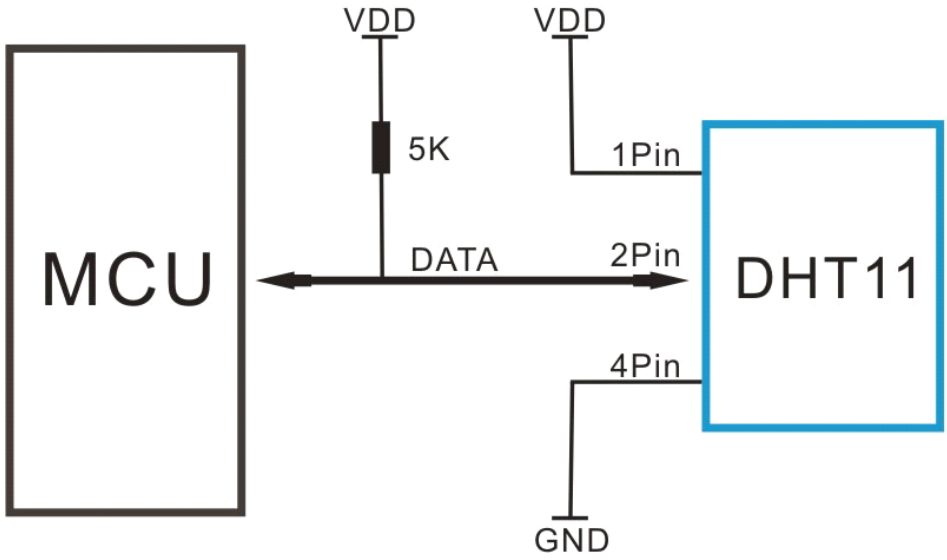


Figure 1 Typical Application

Note: 3Pin – Null; MCU = Micro-computer Unite or single chip Computer

When the connecting cable is shorter than 20 metres, a 5K pull-up resistor is recommended; when the connecting cable is longer than 20 metres, choose a appropriate pull-up resistor as needed.

4. Power and Pin

DHT11's power supply is 3-5.5V DC. When power is supplied to the sensor, do not send any instruction to the sensor in within one second in order to pass the unstable status. One capacitor valued 100nF can be added between VDD and GND for power filtering.

5. Communication Process: Serial Interface (Single-Wire Two-Way)

Single-bus data format is used for communication and synchronization between MCU and DHT11 sensor. One communication process is about 4ms.

Data consists of decimal and integral parts. A complete data transmission is **40bit**, and the sensor sends **higher data bit** first.

Data format: 8bit integral RH data + 8bit decimal RH data + 8bit integral T data + 8bit decimal T data + 8bit check sum. If the data transmission is right, the check-sum should be the last 8bit of "8bit integral RH data + 8bit decimal RH data + 8bit integral T data + 8bit decimal T data".

5.1 Overall Communication Process (Figure 2, below)

When MCU sends a start signal, DHT11 changes from the low-power-consumption mode to the running-mode, waiting for MCU completing the start signal. Once it is completed, DHT11 sends a response signal of 40-bit data that include the relative humidity and temperature information to MCU. Users can choose to collect (read) some data. Without the start signal from MCU, DHT11 will not give the response signal to MCU. Once data is collected, DHT11 will change to the low-power-consumption mode until it receives a start signal from MCU again.

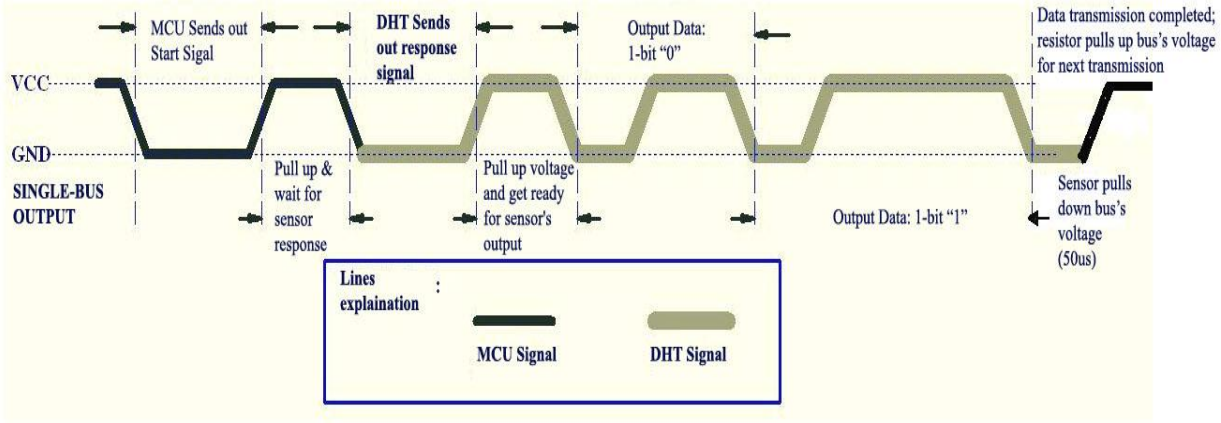


Figure 2 Overall Communication Process

5.2 MCU Sends out Start Signal to DHT (Figure 3, below)

Data Single-bus free status is at high voltage level. When the communication between MCU and DHT11 begins, the programme of MCU will set Data Single-bus voltage level from high to low and this process must take at least 18ms to ensure DHT's detection of MCU's signal, then MCU will pull up voltage and wait 20-40us for DHT's response.

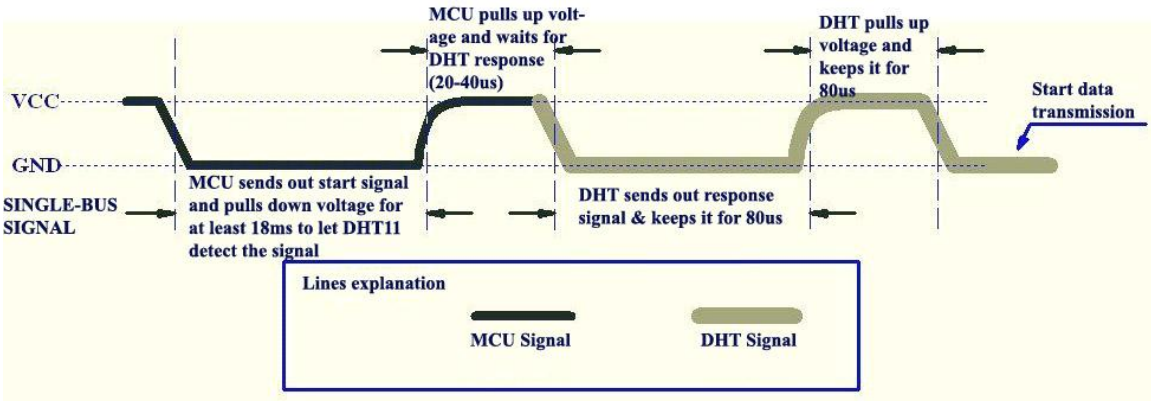


Figure 3 MCU Sends out Start Signal & DHT Responses

5.3 DHT Responses to MCU (Figure 3, above)

Once DHT detects the start signal, it will send out a low-voltage-level response signal, which lasts 80us. Then the programme of DHT sets Data Single-bus voltage level from low to high and keeps it for 80us for DHT's preparation for sending data.

When DATA Single-Bus is at the low voltage level, this means that DHT is sending the response signal. Once DHT sent out the response signal, it pulls up voltage and keeps it for 80us and prepares for data transmission.

When DHT is sending data to MCU, every bit of data begins with the 50us low-voltage-level and the length of the following high-voltage-level signal determines whether data bit is "0" or "1" (see Figures 4 and 5 below).

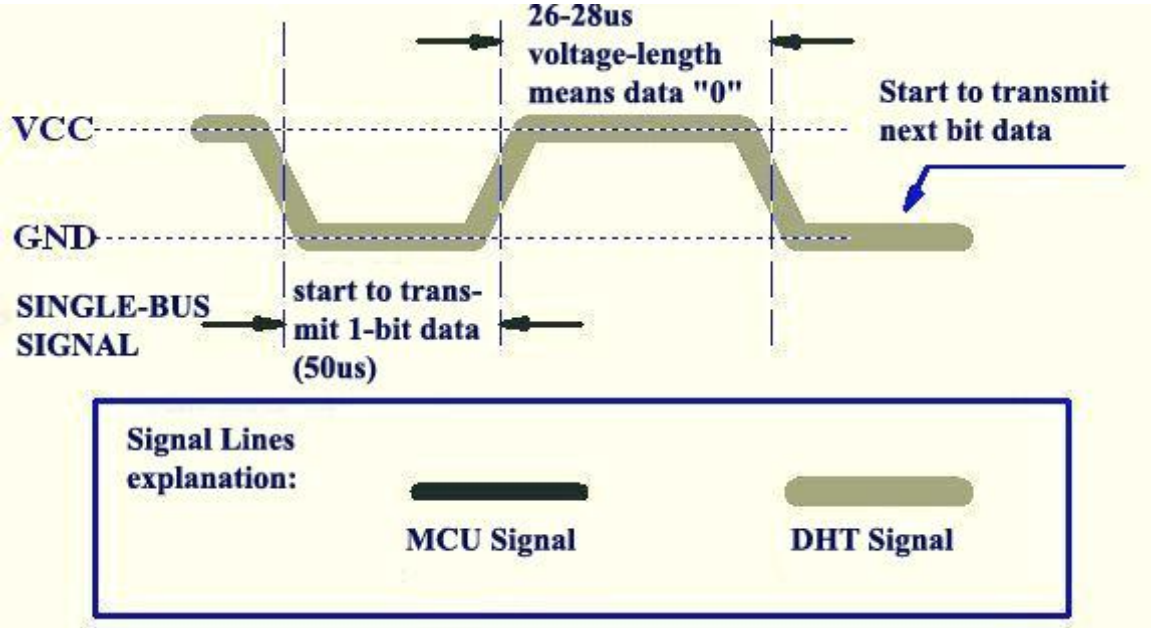


Figure 4 Data "0" Indication

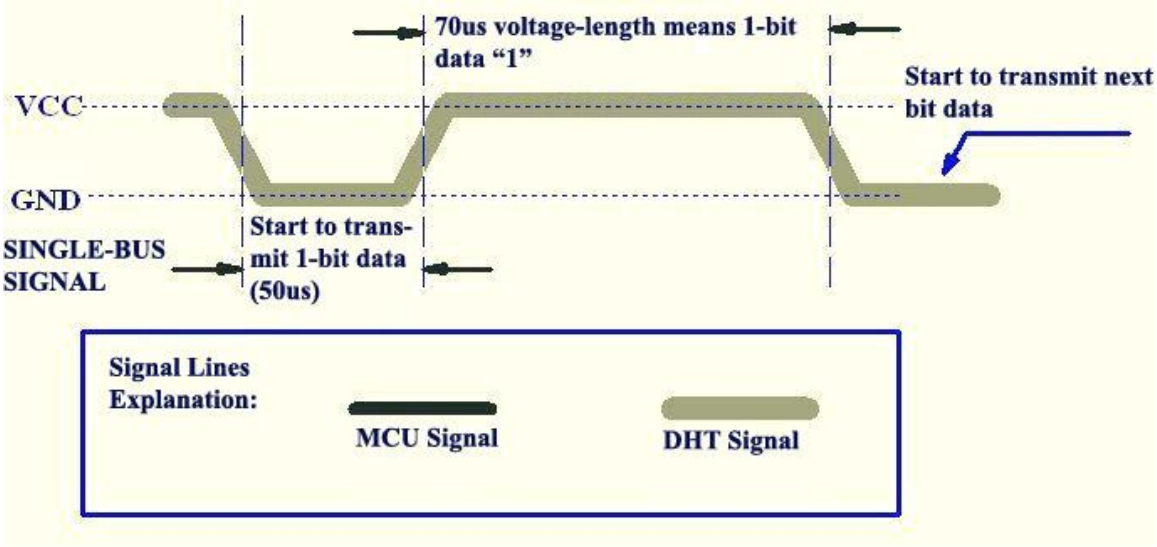


Figure 5 Data "1" Indication

If the response signal from DHT is always at high-voltage-level, it suggests that DHT is not responding properly and please check the connection. When the last bit data is transmitted, DHT11 pulls down the voltage level and keeps it for 50us. Then the Single-Bus voltage will be pulled up by the resistor to set it back to the free status.

6. Electrical Characteristics

VDD=5V, T = 25℃ (unless otherwise stated)

	Conditions	Minimum	Typical	Maximum
Power Supply	DC	3V	5V	5.5V
Current Supply	Measuring	0.5mA		2.5mA
	Average	0.2mA		1mA
	Standby	100uA		150uA
Sampling period	Second	1		

Note: Sampling period at intervals should be no less than 1 second.

7. Attentions of application

(1) Operating conditions

Applying the DHT11 sensor beyond its working range stated in this datasheet can result in 3%RH signal shift/discrepancy. The DHT11 sensor can recover to the calibrated status gradually when it gets back to the normal operating condition and works within its range. Please refer to (3) of

this section to accelerate its recovery. Please be aware that operating the DHT11 sensor in the non-normal working conditions will accelerate sensor's aging process.

(2) Attention to chemical materials

Vapor from chemical materials may interfere with DHT's sensitive-elements and debase its sensitivity. A high degree of chemical contamination can permanently damage the sensor.

(3) Restoration process when (1) & (2) happen

Step one: Keep the DHT sensor at the condition of Temperature 50~60Celsius, humidity <10%RH for 2 hours;
Step two:K keep the DHT sensor at the condition of Temperature 20~30Celsius, humidity >70%RH for 5 hours.

(4) Temperature Affect

Relative humidity largely depends on temperature. Although temperature compensation technology is used to ensure accurate measurement of RH, it is still strongly advised to keep the humidity and temperature sensors working under the same temperature. DHT11 should be mounted at the place as far as possible from parts that may generate heat.

(5) Ligh t Affect

Long time exposure to strong sunlight and ultraviolet may debase DHT's performance.

(6) Connection wires

The quality of connection wires will affect the quality and distance of communication and high quality shielding-wire is recommended.

(7) Other attentions

* Welding temperature should be bellow 260Celsius and contact should take less than 10 seconds.
* Avoid using the sensor under dew condition.
* Do not use this product in safety or emergency stop devices or any other occasion that failure of DHT11 may cause personal injury.
* Storage: Keep the sensor at temperature 10-40℃, humidity <60%RH.

Disclaimer

This is a translated version of the manufacturer's data sheet. OSEPP is not responsible for the accuracy of the translated information.

ESD441 1-Channel ±30kV Unidirectional ESD Diode in an 0201 and 0402 Package

1 Features

- IEC 61000-4-2 level 4 ESD protection
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection
  - 6A (8/20µs)
- IO capacitance:
  - 1pF (typical)
- DC breakdown voltage: 7V (typical)
- Ultra low leakage current: 50nA (maximum)
- Extremely low ESD clamping voltage
  - 7.6V at 16A TLP
  - R_{DYN}: 0.1Ω (I/O to GND)
- Low insertion loss: 2GHz (–3dB bandwidth)
- Supports high speed interfaces up to 4Gbps
- Industrial temperature range: –55°C to +150°C
- Space-saving industry standard 0201 footprint (0.6mm × 0.3mm) and 0402 footprint (1.0mm × 0.6mm)

2 Applications

- End equipment:
  - Vacuum robots
  - Wearables
  - Smart speakers
  - Portable electronics
  - Small appliances
  - Retail automation and payment
  - Laptops and desktops
  - TV and monitors
  - Docking stations
- Interfaces:
  - USB 2.0
  - HDMI™ 1.4 and 2.0
  - DisplayPort™
  - SIM card
  - GPIO

3 Description

The ESD441 is a unidirectional ESD protection diode for protecting data lines and other I/O ports. The ESD441 is rated to dissipate ESD strikes up to ±30kV per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 1pF (typical) IO capacitance enabling high-speed interfaces protection for protocols such as USB 2.0. The extremely low dynamic resistance (0.1Ω) and clamping voltage (7.6V at 16TLP) is specified for system level protection against transient events.

The 30kV ESD rating and 6A surge provides robust transient protection in a tiny package for protecting 5.5V power rails in portable electronics and other space constrained applications such as wearables.

The ESD441 is offered in the industry standard 0201 and 0402 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD441	DPL (DFN0603, 2)	0.6mm × 0.3mm
	DPY (DFN1006, 2)	1.0mm × 0.6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

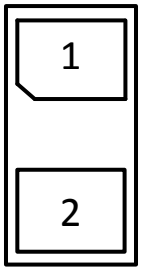


Figure 4-1. DPL Package, 2-Pin DFN0603 (Top View)

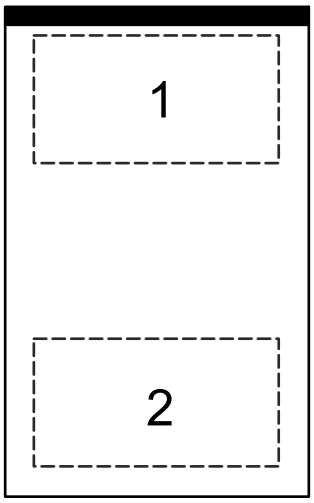


Figure 4-2. DPY Package, 2-Pin DFN1006 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected channel
GND	2	GND	Ground. Connect to ground.

(1) I = input, O = output, GND = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Peak Pulse (2) (3)	IEC 61000-4-5 power (t_p - 8/20 µs)		45	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		6	A
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

5.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002 (2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufactuuring with a standard ESD control proccess.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufactuuring with a standard ESD control proccess.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	IO to GND	0		5.5	V
T_A	Operating free-air temperature		-55		150	°C

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5.5 Thermal Information

THERMAL METRIC (1)		ESD441		UNIT
		DPL (DFN0603)	DPY (DFN1006)	
		2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	519.9	448.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	336.9	308.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	209.2	197.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	136.7	159.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	207.2	196.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.6 Electrical Characteristics

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		PACKAGE	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	DPL & DPY package	I_{IO} <100nA, across operating temperature range			5.5	V
I_{LEAK}	Reverse leakage current		V_{IO} = 5.5V, IO to GND or GND to IO		1	50	nA
V_{BR}	Break-down voltage		I_{IO} = 1mA, IO to GND	6	7	8	V
V_{CLAMP}	Clamping voltage with TLP	DPL Package	I_{PP} = 1A, TLP, IO to GND		6.3		V
			I_{PP} = 5A, TLP, IO to GND		6.5		
			I_{PP} = 16A, TLP, IO to GND		7.6		
			I_{PP} =16A, TLP, GND to IO		3.8		
	Clamping voltage with surge strike (3)		I_{PP} = 6A, t_p = 8/20 µs , IO to GND		7.6		
R_{DYN}	Dynamic resistance (2)	DPL Package	IO to GND		0.1		Ω
			GND to IO		0.16		
V_{CLAMP}	Clamping voltage with TLP	DPY Package	I_{PP} = 1A, TLP, IO to GND		7.1		V
			I_{PP} = 5A, TLP, IO to GND		7.3		
			I_{PP} = 16A, TLP, IO to GND		8.2		
			I_{PP} =16A, TLP, GND to IO		3.8		
	Clamping voltage with surge strike (3)		I_{PP} = 6A, t_p = 8/20µs , IO to GND		8.6		
R_{DYN}	Dynamic resistance (2)	DPY Package	IO to GND		0.16		Ω
			GND to IO		0.16		
C_L	Line capacitance	DPL & DPY Package	V_{IO} = 0V; f = 1MHz, V_{pp} = 30mV, IO to GND or IO to GND		1		pF

(1) Typical parameters are measured at 25℃
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10A and I = 20A
(3) Nonrepetitive current pulse 8 to 20µs exponentially decaying waveform according to IEC 61000-4-5

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5.7 Typical Characteristics

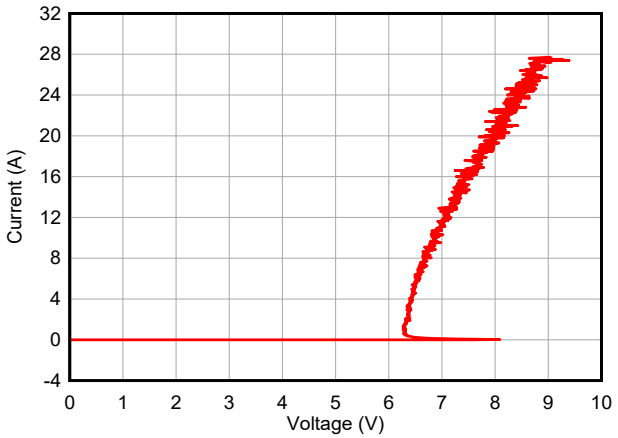


Figure 5-1. Positive TLP Curve (DPL)

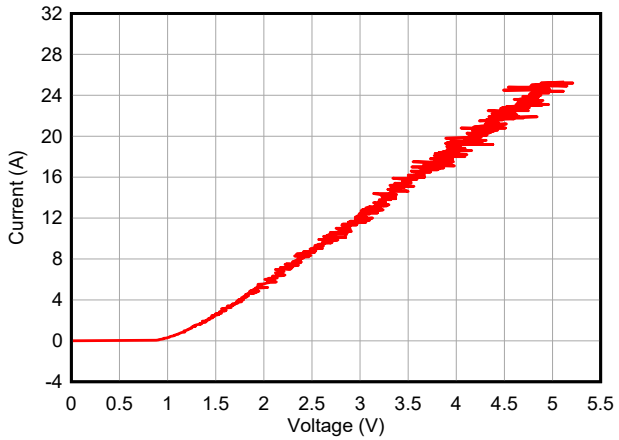


Figure 5-2. Negative TLP Curve (DPL)

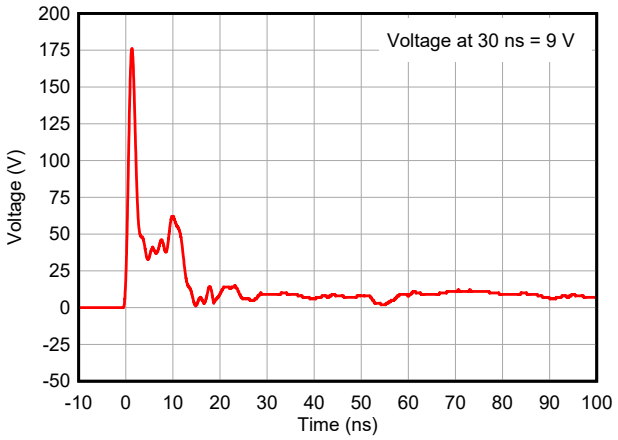


Figure 5-3. +8kV Clamped IEC Waveform (DPL)

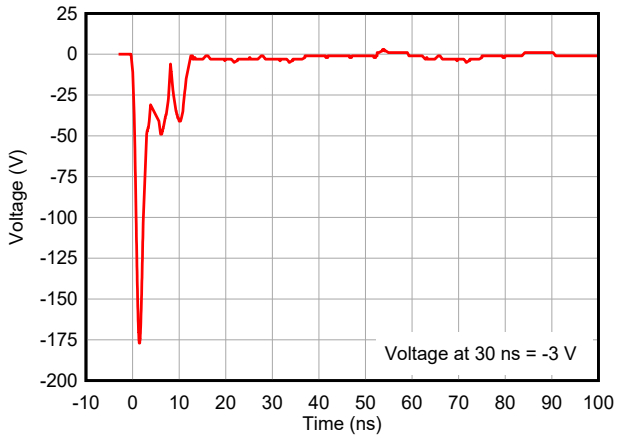


Figure 5-4. -8kV Clamped IEC Waveform (DPL)

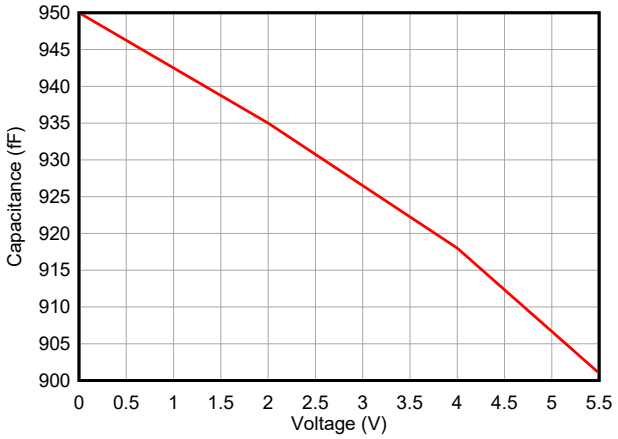


Figure 5-5. Bias Voltage vs. Capacitance (DPL)

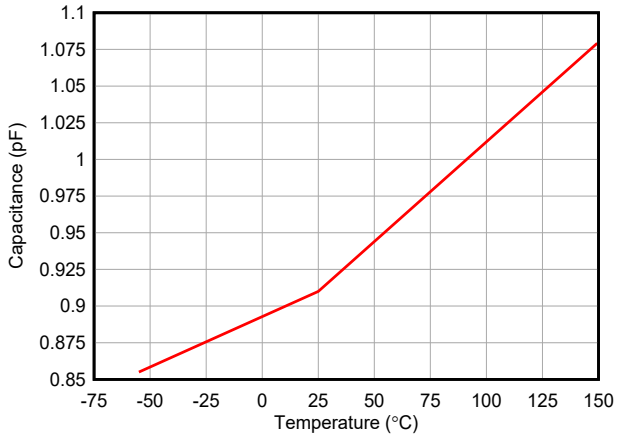


Figure 5-6. Temperature vs. Capacitance (DPL)

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5.7 Typical Characteristics (continued)

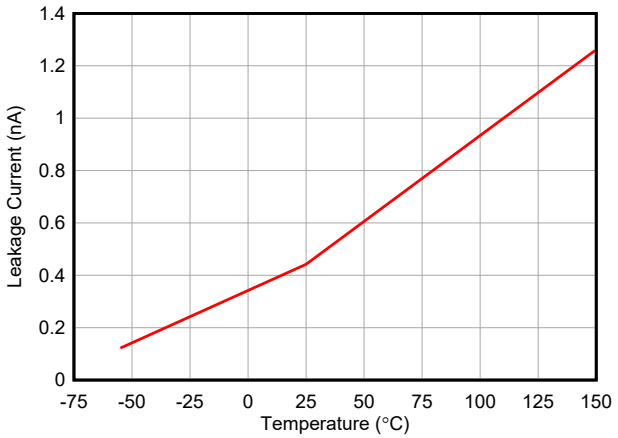


Figure 5-7. Temperature vs. Leakage Current (DPL)

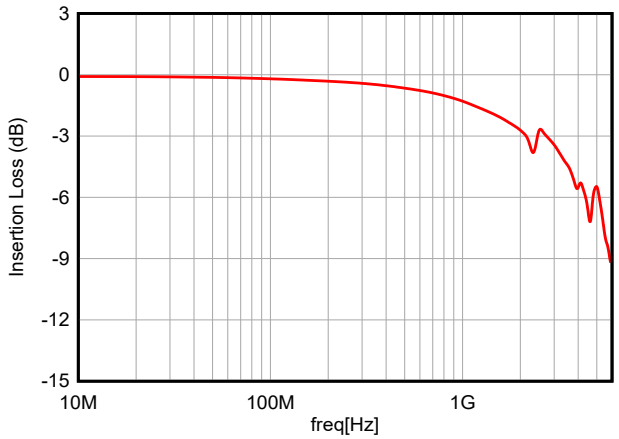


Figure 5-8. Insertion Loss (DPL)

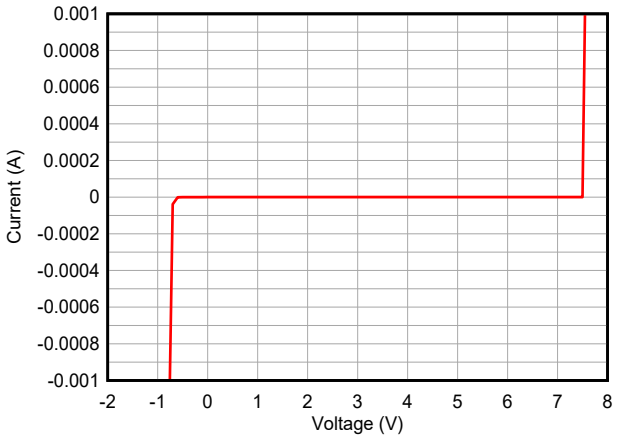


Figure 5-9. DC I-V Curve (DPL)

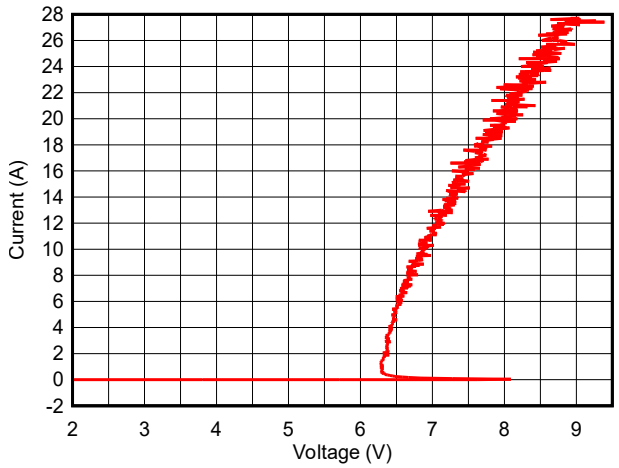


Figure 5-10. Positive TLP Curve (DPY)

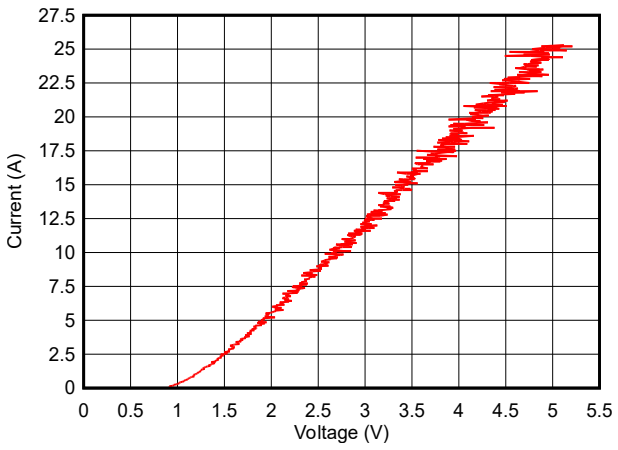


Figure 5-11. Negative TLP Curve (DPY)

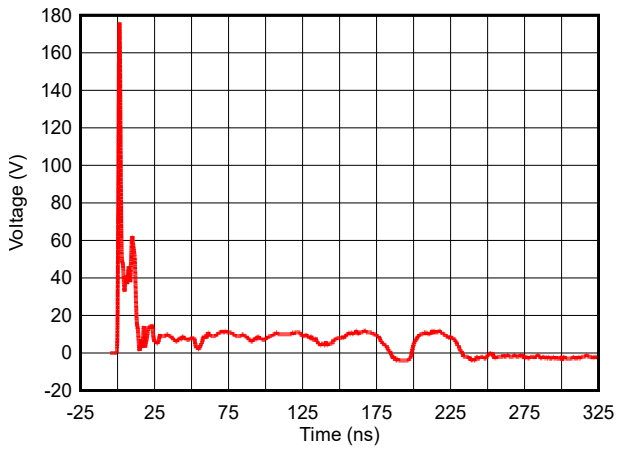


Figure 5-12. +8kV Clamped IEC Waveform (DPY)

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5.7 Typical Characteristics (continued)

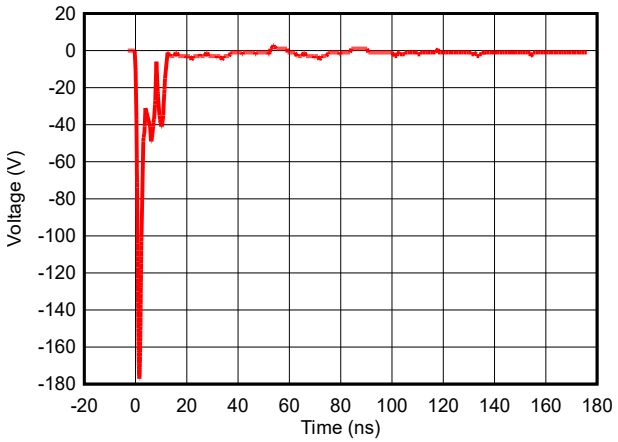


Figure 5-13. -8kV Clamped IEC Waveform (DPY)

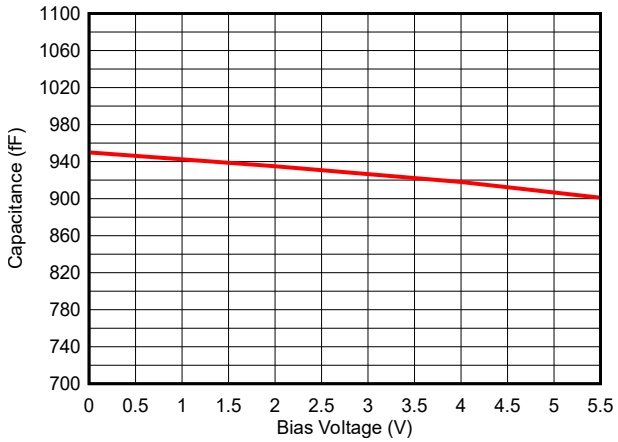


Figure 5-14. Bias Voltage vs. Capacitance (DPY)

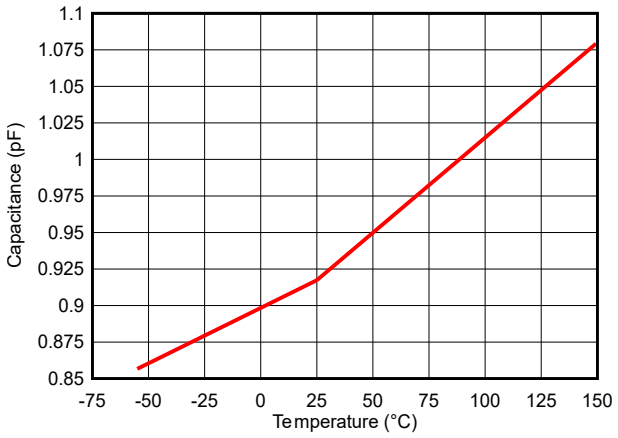


Figure 5-15. Temperature vs. Capacitance (DPY)

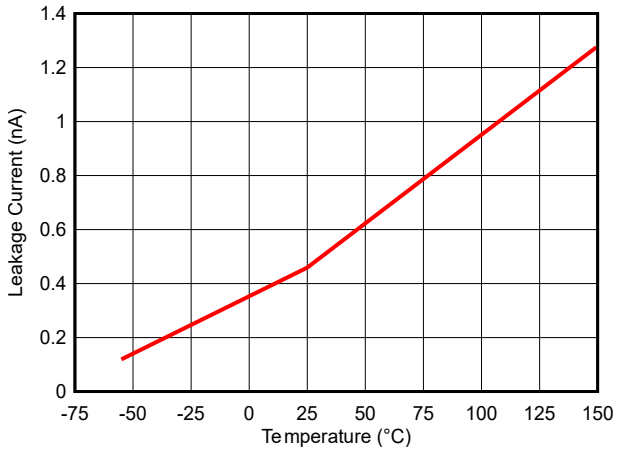


Figure 5-16. Temperature vs. Leakage Current (DPY)

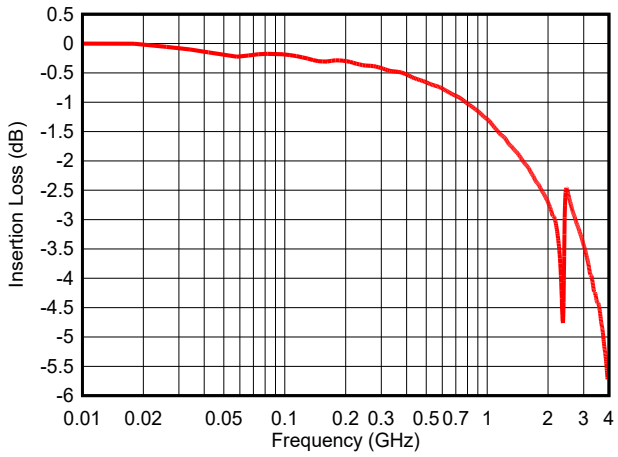


Figure 5-17. Insertion Loss (DPY)

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD441 is a diode type TVS which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, please refer to the *ESD Packaging and Layout Guide* for details.

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7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide*
- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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DisplayPort™ is a trademark of Video Electronics Standards Association.
TI E2E™ is a trademark of Texas Instruments.
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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2025) to Revision C (September 2026)	Page
• Changed min input pin voltage from -5.5V to 0V	4
• Removed 5.5V VRWM min limit	6

Changes from Revision A (June 2023) to Revision B (December 2025)	Page
• Added DPY package throughout the data sheet	1

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD441DPLR	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E
ESD441DPLR.B	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E
ESD441DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

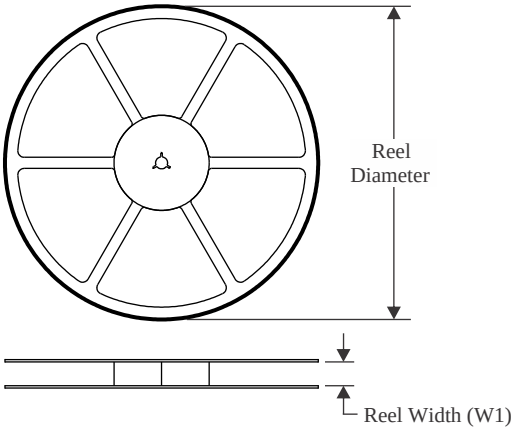
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

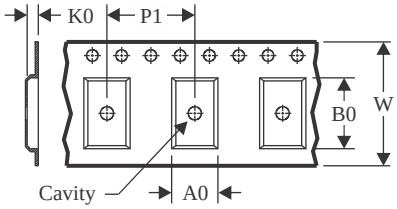
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

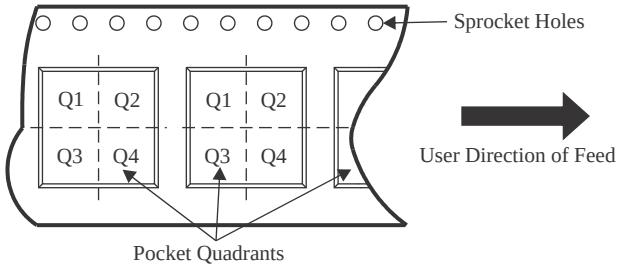


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

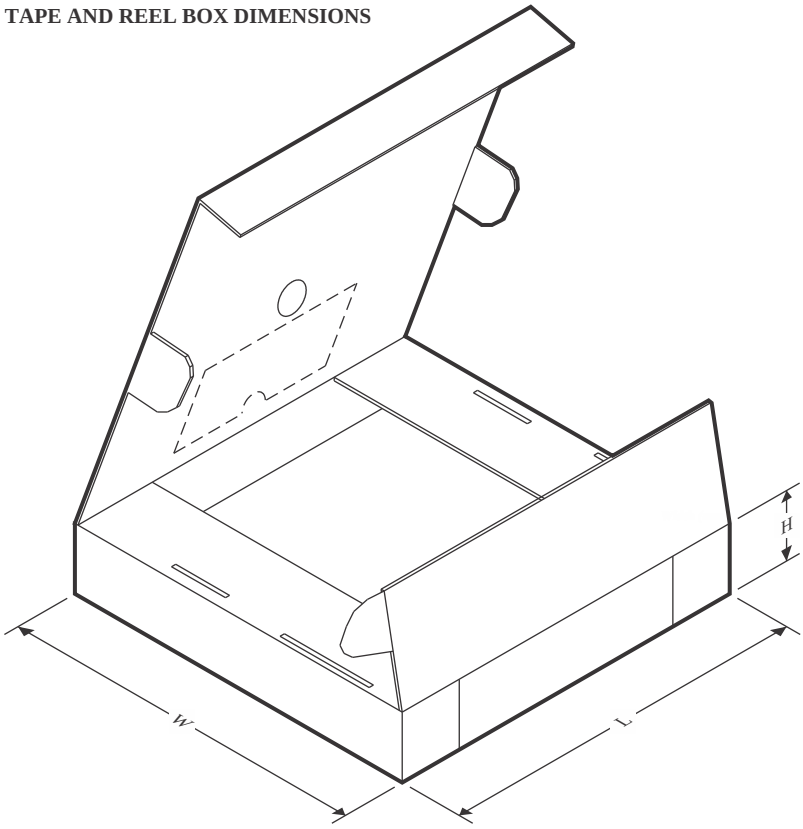
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD441DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
ESD441DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD441DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0
ESD441DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



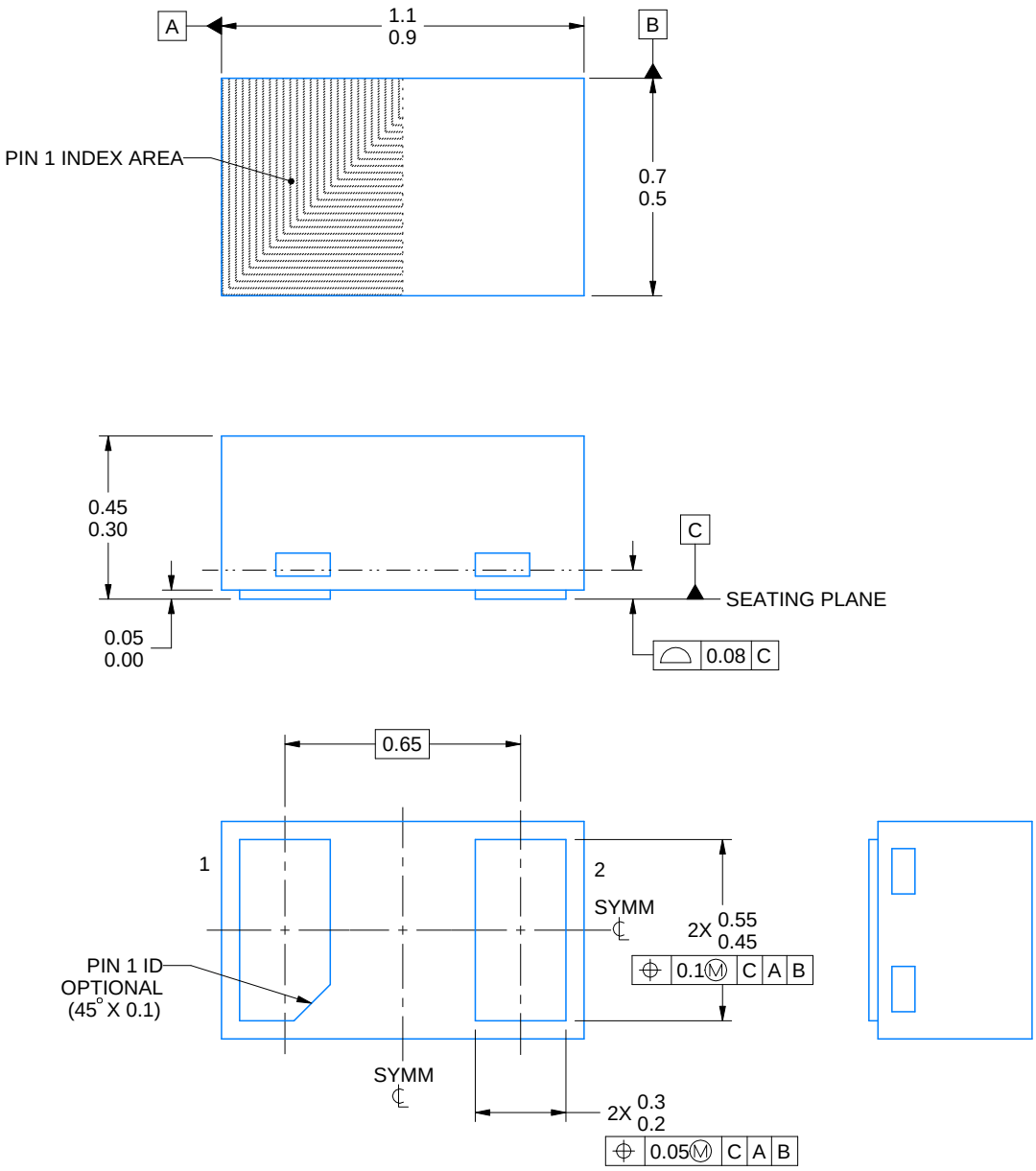
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

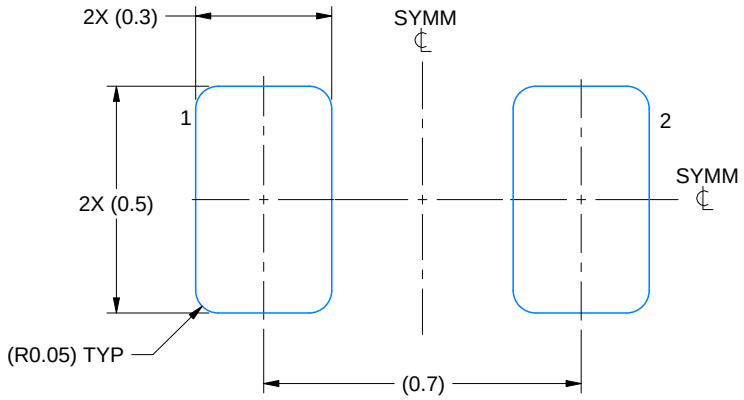
PLASTIC SMALL OUTLINE - NO LEAD



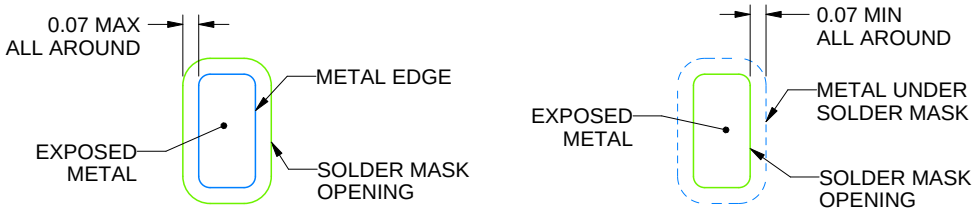
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

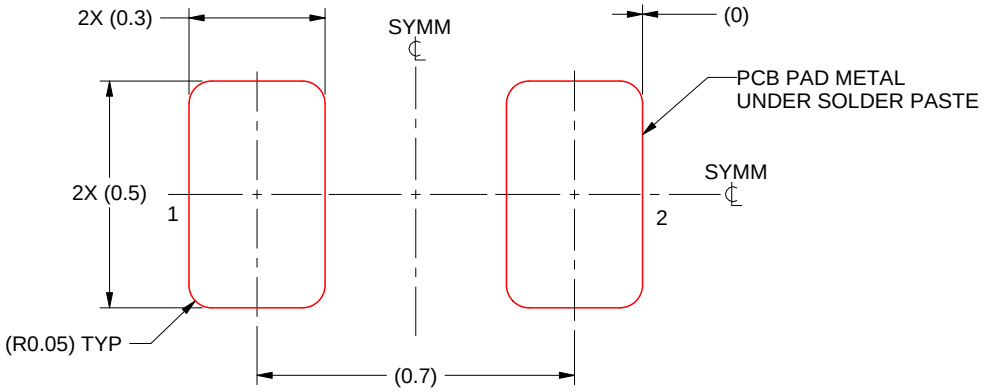


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



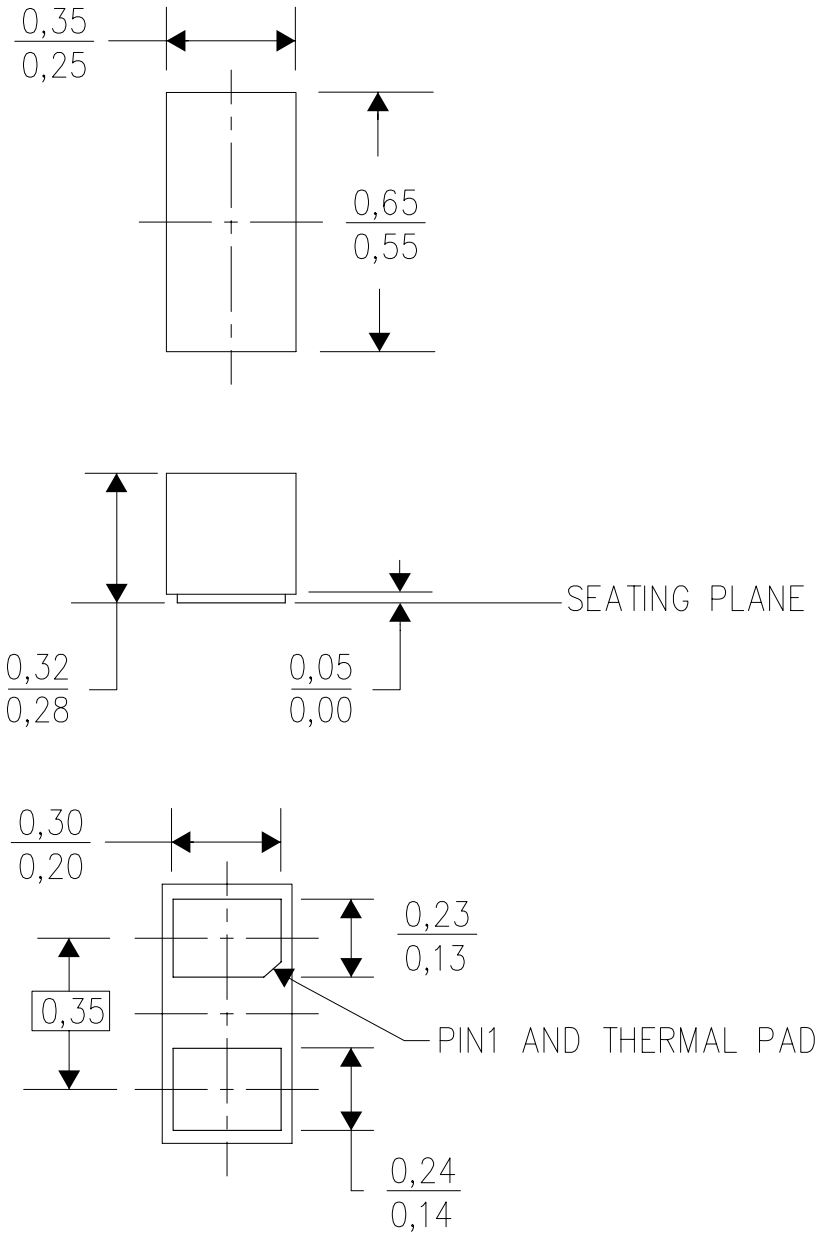
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

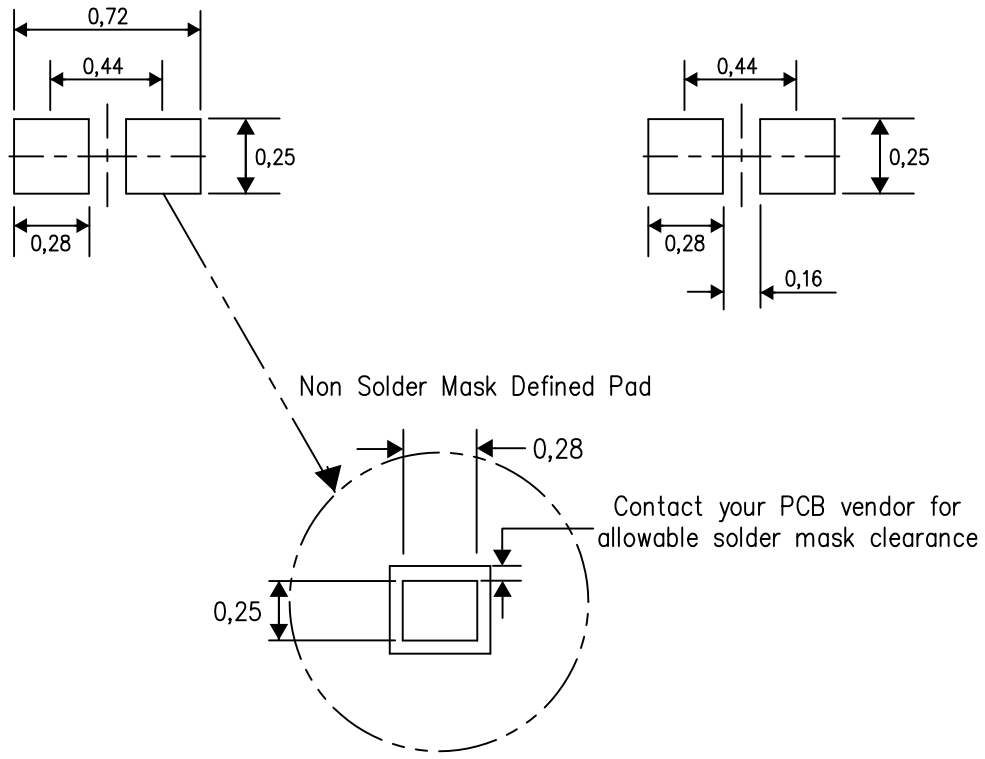


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Last updated 10/2025

ESP32-C6-WROOM-1
ESP32-C6-WROOM-1U

Datasheet Version 1.4

Module that supports 2.4 GHz Wi-Fi 6 (802.11ax), Bluetooth® 5 (LE), Zigbee and Thread (802.15.4)
Built around ESP32-C6 series of SoCs, 32-bit RISC-V single-core microprocessor
Flash up to 8 MB
23 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector



ESP32-C6-WROOM-1



ESP32-C6-WROOM-1U

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-c6-wroom-1_wroom-1u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-C6 embedded, 32-bit RISC-V single-core microprocessor, up to 160 MHz
- ROM: 320 KB
- HP SRAM: 512 KB
- LP SRAM: 16 KB

Wi-Fi

- 1T1R in 2.4 GHz band
- Operating frequency: 2412 ~ 2484 MHz
- IEEE 802.11ax-compliant
  - 20 MHz-only non-AP mode
  - MCS0 ~ MCS9
  - Uplink and downlink OFDMA, especially suitable for simultaneous connections in high-density environments
  - Downlink MU-MIMO (multi-user, multiple input, multiple output) to increase network capacity
  - Beamformee that improves signal quality
  - Channel quality indication (CQI)
  - DCM (dual carrier modulation) to improve link robustness
  - Spatial reuse to maximize parallel transmissions
  - Target wake time (TWT) that optimizes power saving mechanisms
- Fully compatible with IEEE 802.11b/g/n protocol
  - 20 MHz and 40 MHz bandwidth
  - Data rate up to 150 Mbps
  - Wi-Fi Multimedia (WMM)
  - TX/RX A-MPDU, TX/RX A-MSDU
  - Immediate Block ACK
  - Fragmentation and defragmentation
  - Transmit opportunity (TXOP)
  - Automatic Beacon monitoring (hardware TSF)
  - 4 × virtual Wi-Fi interfaces
  - Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode *Note that when ESP32-C6 scans in Station mode, the SoftAP channel will change along with the Station channel*
  - 802.11mc FTM

Bluetooth®

- Bluetooth LE: Bluetooth 5.3 certified
- Bluetooth mesh
- High power mode (20 dBm)
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- LE power control

- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

IEEE 802.15.4

- Compliant with IEEE 802.15.4-2015 protocol
- OQPSK PHY in 2.4 GHz band
- Data rate: 250 Kbps
- Thread 1.3
- Zigbee 3.0

Peripherals

- GPIO, SPI, parallel IO interface, UART, I2C, I2S, RMT (TX/RX), pulse counter, LED PWM, USB Serial/JTAG controller, MCPWM, SDIO slave controller, GDMA, TWAI® controller, on-chip debug functionality via JTAG, event task matrix, ADC, temperature sensor, system timer, general-purpose timers, and watchdog timers

Integrated Components on Module

- 40 MHz crystal oscillator
- SPI flash

Antenna Options

- On-board PCB antenna (ESP32-C6-WROOM-1)
- External antenna via a connector (ESP32-C6-WROOM-1U)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C

Certification

- RF certification: See certificates
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Series Comparison

ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U are two powerful, general-purpose Wi-Fi, IEEE 802.15.4, and Bluetooth LE modules. The rich set of peripherals and high performance make the module an ideal choice for smart homes, industrial automation, health care, consumer electronics, etc.

ESP32-C6-WROOM-1 comes with a PCB antenna. ESP32-C6-WROOM-1U comes with a connector for an external antenna. They both feature an external SPI flash up to 8 MB.

Both ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U come in two versions:

- 4 MB flash version
- 8 MB flash version

The two versions only vary in flash part number. In this datasheet unless otherwise stated, ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U refer to the variants in 4 MB and 8 MB flash versions.

The series comparison for the two modules is as follows:

Table 1-1. ESP32-C6-WROOM-1 (ANT) Series Comparison[1]

Part Number	Flash[2,3]	Ambient Temp.[4] (°C)	Size[5] (mm)
ESP32-C6-WROOM-1-N4	4 MB (Quad SPI)	−40 ~ 85	18.0 × 25.5 × 3.1
ESP32-C6-WROOM-1-N8	8 MB (Quad SPI)		
ESP32-C6-WROOM-1-N16	16 MB (Quad SPI)		

[1] This table shares the same notes presented in Table 1-2 below.

Table 1-2. ESP32-C6-WROOM-1U (CONN) Series Comparison

Part Number	Flash[2,3]	Ambient Temp.[4] (°C)	Size[5] (mm)
ESP32-C6-WROOM-1U-N4	4 MB (Quad SPI)	−40 ~ 85	18.0 × 19.2 × 3.2
ESP32-C6-WROOM-1U-N8	8 MB (Quad SPI)		
ESP32-C6-WROOM-1U-N16	16 MB (Quad SPI)		

[2] For specifications, refer to Section 6.5 *Memory Specifications*.

[3] By default, the SPI flash on the module operates at a maximum clock frequency of 80 MHz and does not support the auto suspend feature. If you need the flash auto suspend feature, please contact us.

[4] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[5] For details, refer to Section 10.1 *Physical Dimensions*.

At the core of the modules is ESP32-C6, a 32-bit RISC-V single-core processor.

Note:
For more information on ESP32-C6, please refer to *ESP32-C6 Series Datasheet*.

Please contact our sales team if you require modules with 4 MB flash and maximum ambient temperature of 105 °C.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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2 Block Diagram

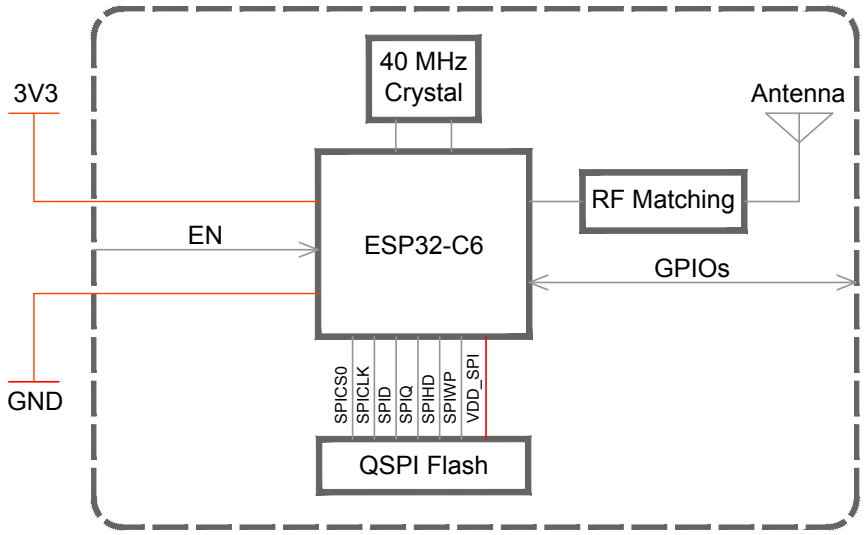


Figure 2-1. ESP32-C6-WROOM-1 Block Diagram

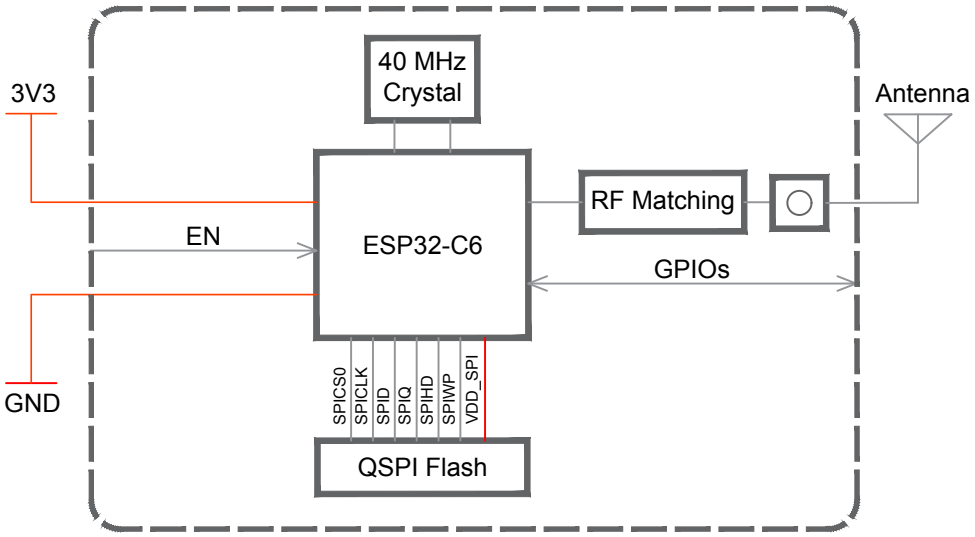


Figure 2-2. ESP32-C6-WROOM-1U Block Diagram

Note:
For the pin mapping between the chip and the in-package flash, please refer to *ESP32-C6 Series Datasheet* > Table *Pin Mapping Between Chip and Flash*.

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Physical Dimensions*.

The pin diagram is applicable for ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U, but the latter has no keepout zone.

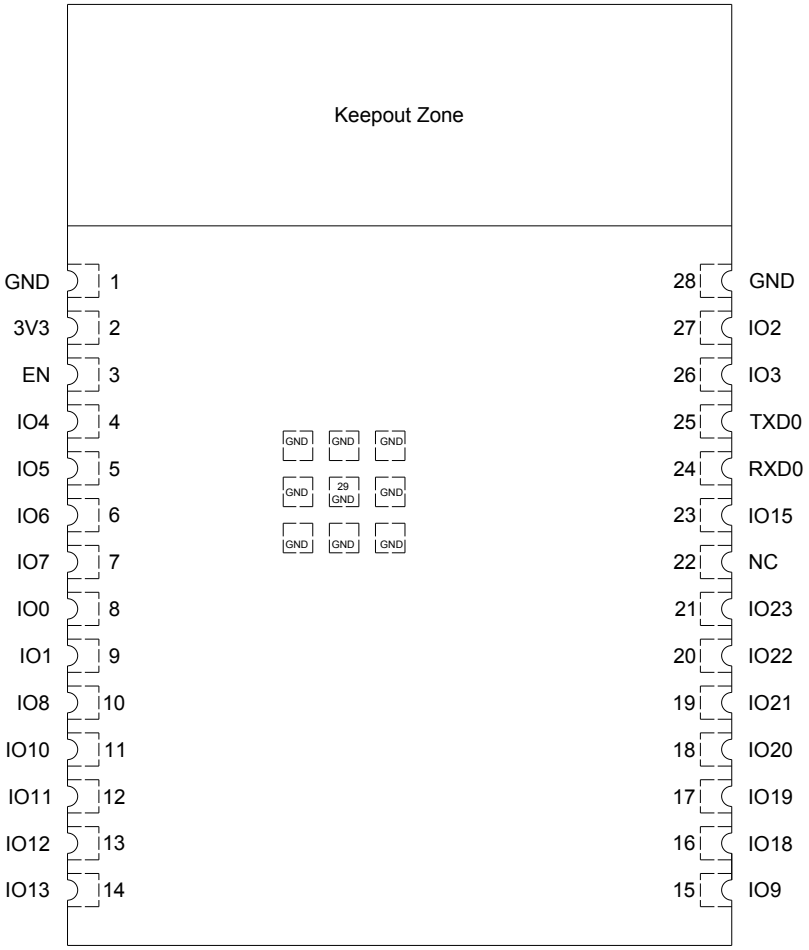


Figure 3-1. Pin Layout (Top View)

3.2 Pin Description

The module has 29 pins. See pin definitions in Table 3-1 *Pin Definitions*.

Table 3-1. Pin Definitions

Name	No.	Type[1]	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	MTMS, GPIO4, LP_GPIO4, LP_UART_RXD, ADC1_CH4, FSPIHD
IO5	5	I/O/T	MTDI, GPIO5, LP_GPIO5, LP_UART_TXD, ADC1_CH5, FSPIWP
IO6	6	I/O/T	MTCK, GPIO6, LP_GPIO6, LP_I2C_SDA, ADC1_CH6, FSPICLK
IO7	7	I/O/T	MTDO, GPIO7, LP_GPIO7, LP_I2C_SCL, FSPID
IO0	8	I/O/T	GPIO0, XTAL_32K_P, LP_GPIO0, LP_UART_DTRN, ADC1_CH0
IO1	9	I/O/T	GPIO1, XTAL_32K_N, LP_GPIO1, LP_UART_DSRN, ADC1_CH1
IO8	10	I/O/T	GPIO8
IO10	11	I/O/T	GPIO10
IO11	12	I/O/T	GPIO11
IO12	13	I/O/T	GPIO12, USB_D-
IO13	14	I/O/T	GPIO13, USB_D+
IO9	15	I/O/T	GPIO9
IO18	16	I/O/T	GPIO18, SDIO_CMD, FSPICS2
IO19	17	I/O/T	GPIO19, SDIO_CLK, FSPICS3
IO20	18	I/O/T	GPIO20, SDIO_DATA0, FSPICS4
IO21	19	I/O/T	GPIO21, SDIO_DATA1, FSPICS5
IO22	20	I/O/T	GPIO22, SDIO_DATA2
IO23	21	I/O/T	GPIO23, SDIO_DATA3
NC	22	—	NC
IO15	23	I/O/T	GPIO15
RXD0	24	I/O/T	U0RXD, GPIO17, FSPICS1
TXD0	25	I/O/T	U0TXD, GPIO16, FSPICS0
IO3	26	I/O/T	GPIO3, LP_GPIO3, LP_UART_CTSN, ADC1_CH3
IO2	27	I/O/T	GPIO2, LP_GPIO2, LP_UART_RTSN, ADC1_CH2, FSPIQ
GND	28	P	Ground
EPAD	29	P	Ground

[1] P: power supply; I: input; O: output; T: high impedance.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-C6 Series Datasheet* > Chapter *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse parameters at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO8 and GPIO9
- **SDIO Sampling and Driving Clock Edge**
  - Strapping pin: MTMS and MTDI
- **ROM message printing**
  - Strapping pin: GPIO8
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- **JTAG signal source**
  - Strapping pin: GPIO15
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP32-C6 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
MTMS	Floating	–
MTDI	Floating	–
GPIO8	Floating	–
GPIO9	Weak pull-up	1
GPIO15	Floating	–

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-C6 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At Chip Reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in

any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset. For details on Chip Reset, see *ESP32-C6 Technical Reference Manual* > Chapter *Reset and Clock*.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 4-2 and Figure 4-1.

Table 4-2. Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

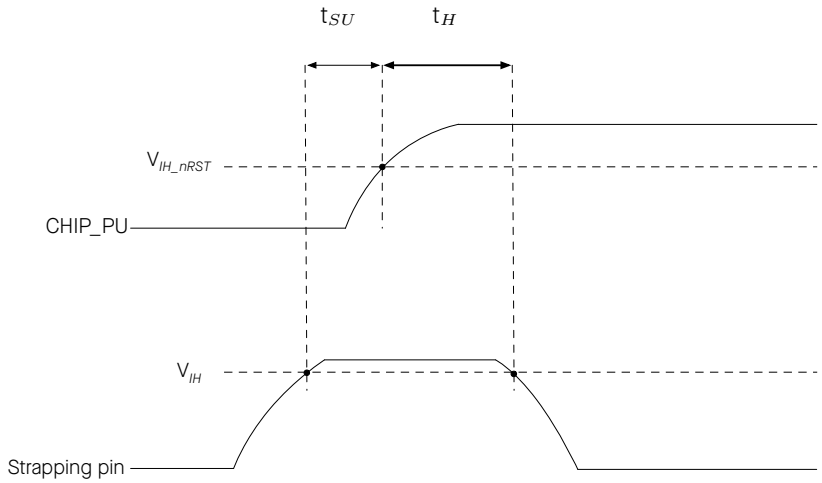


Figure 4-1. Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 4-3 *Chip Boot Mode Control*.

Table 4-3. Chip Boot Mode Control

Boot Mode	GPIO8	GPIO9
SPI boot mode	Any value	**1**
Joint download boot mode [2]	1	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SDIO Download Boot

4.2 SDIO Sampling and Driving Clock Edge Control

The strapping pin MTMS and MTDI can be used to decide on which clock edge to sample signals and drive output lines. See Table 4-4 *SDIO Input Sampling Edge/Output Driving Edge Control*.

Table 4-4. SDIO Input Sampling Edge/Output Driving Edge Control

Edge behavior	MTMS	MTDI
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	1	1

[1] MTMS and MTDI are floating by default, so above are not default configurations.

4.3 ROM Messages Printing Control

During the boot process, ROM message printing is enabled if LP_AON_STORE4_REG[0] is 0 (default), and disabled if LP_AON_STORE4_REG[0] is 1. When ROM message printing is enabled, the messages can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table 4-5 *UART0 ROM Message Printing Control*.

Table 4-5. UART0 ROM Message Printing Control

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8
Enabled	**0**	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

[1] **Bold** marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to **USB Serial/JTAG controller** as shown in Table 4-6 *USB Serial/JTAG ROM Message Printing Control*.

Table 4-6. USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Code Printing	EFUSE_DIS_USB_SERIAL_JTAG [2]	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled	**0**	**0**
Disabled	0	1
	1	Ignored

[1] **Bold** marks the default value and configuration.

[2] EFUSE_DIS_USB_SERIAL_JTAG controls whether to disable USB Serial/JTAG.

4.4 JTAG Signal Source Control

The strapping pin GPIO15 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 4-7 *JTAG Signal Source Control* shows, GPIO15 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG and EFUSE_JTAG_SEL_ENABLE.

Table 4-7. JTAG Signal Source Control

JTAG Signal Source	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_JTAG_SEL_ENABLE	GPIO15
USB Serial/JTAG Controller	**0**	**0**	**0**	Ignored
	0	0	1	1
	1	0	Ignored	Ignored
JTAG pins [2]	0	0	1	0
	0	1	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

[1] **Bold** marks the default value and configuration.

[2] JTAG pins refer to MTDI, MTCK, MTMS, and MTDO.

4.5 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails need a short time to stabilize. After that, CHIP_PU – the pin used for power-up and reset – is pulled high to activate the chip. For information on CHIP_PU as well as power-up and reset timing, see Figure 4-2 and Table 4-8.

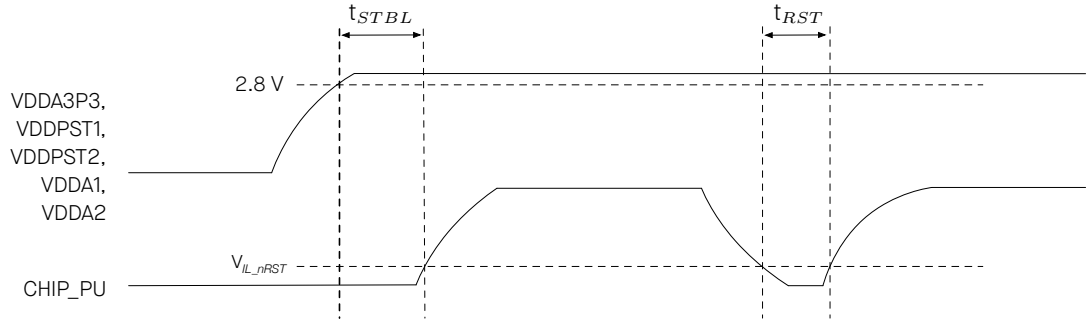


Figure 4-2. Visualization of Timing Parameters for Power-up and Reset

Table 4-8. Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDA3P3, VDDPST1, VDDPST2, VDDA1 and VDDA2 to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip (see Table 6-3)	50

5 Peripherals

5.1 Functional Overview

ESP32-C6 integrates a rich set of peripherals including SPI, parallel IO interface, UART, I2C, I2S, RMT (TX/RX), LED PWM, USB Serial/JTAG controller, MCPWM, SDIO slave controller, GDMA, TWAI® controller, on-chip debug functionality via JTAG, event task matrix, ADC, as well as up to 23 GPIOs, etc.

For detailed information about module peripherals, please refer to *ESP32-C6 Series Datasheet* > Section *Functional Description*. Note that the ADC measurement range and accuracy in the *ESP32-C6 Series Datasheet* are applicable to modules manufactured on and after the PW Number **PW-2023-07-XXX** on packaging labels. For modules manufactured earlier than these PW numbers, please ask our sales team to provide the actual range and accuracy according to batches.

Note:
The content below is excerpted from *ESP32-C6 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U as not all the IO signals are exposed on the module. To learn more details about peripherals signals, please refer to *ESP32-C6 Technical Reference Manual* > Section *Peripheral Signal List*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

The UART Controller in the ESP32-C6 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It consists of two UARTs in the main system, and one low-power LP UART.

Feature List

- Programmable baud rates up to 5 MBaud
- RAM shared by TX FIFOs and RX FIFOs
- Support for various lengths of data bits and stop bits
- Parity bit support
- Special character AT_CMD detection
- RS485 protocol support (not supported by LP UART)
- IrDA protocol support (not supported by LP UART)

- High-speed data communication using GDMA (not supported by LP UART)
- Receive timeout feature
- UART as the wake-up source
- Software and hardware flow control

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.2 SPI Controller

ESP32-C6 has the following SPI interfaces:

- **SPI0** used by ESP32-C6's cache and GDMA to access in-package or off-package flash
- **SPI1** used by the CPU to access in-package or off-package flash
- **SPI2** is a general-purpose SPI controller with access to general-purpose DMA channels

SPI0 and SPI1 are reserved for system use, and only SPI2 is available for users.

Features of SPI0 and SPI1

- Supports Single SPI, Dual SPI, Quad SPI (QPI) modes
- Data transmission is in bytes

Features of SPI2

- Supports operation as a master or slave
- Support for GDMA
- Supports Single SPI, Dual SPI, Quad SPI (QPI) modes
- Configurable clock polarity (CPOL) and phase (CPHA)
- Configurable clock frequency
- Data transmission is in bytes
- Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
- As a master
  - Supports 2-line full-duplex communication with clock frequency up to 80 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 80 MHz
  - Provides six FSPICS... pins for connection with six independent SPI slaves
  - Configurable CS setup time and hold time
- As a slave
  - Supports 2-line full-duplex communication with clock frequency up to 40 MHz

- Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 40 MHz

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.3 I2C Controller

The I2C Controller supports communication between the master and slave devices using the I2C bus.

Feature List

- Two I2C controllers: one in the main system and one in the low-power system
- Communication with multiple external devices
- Master and slave modes for I2C, and master mode only for LP I2C
- Standard mode (100 Kbit/s) and fast mode (400 Kbit/s)
- SCL clock stretching in slave mode
- Programmable digital noise filtering
- Support for 7-bit and 10-bit addressing, as well as dual address mode

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.4 I2S Controller

The I2S Controller in the ESP32-C6 chip provides a flexible communication interface for streaming digital data in multimedia applications, particularly digital audio applications.

Feature List

- Master mode and slave mode
- Full-duplex and half-duplex communications
- Separate TX and RX units that can work independently or simultaneously
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- PCM-to-PDM TX interface
- Configurable high-precision BCK clock, with frequency up to 40 MHz

  - Sampling frequencies can be 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 128 kHz, 192 kHz, etc.
- 8-/16-/24-/32-bit data communication
- Direct Memory Access (DMA)
- A-law and μ-law compression/decompression algorithms for improved signal-to-quantization noise ratio
- Flexible data format control

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.5 Pulse Count Controller

The Pulse Count Controller (PCNT) is designed to count input pulses by tracking rising and falling edges of the input pulse signal.

Feature List

- Four independent pulse counters with two channels each
- Counter modes: increment, decrement, or disable
- Glitch filtering for input pulse signals and control signals
- Selection between counting on rising or falling edges of the input pulse signal

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.6 USB Serial/JTAG Controller

The USB Serial/JTAG controller in the ESP32-C6 chip provides an integrated solution for communicating to the chip over a standard USB CDC-ACM serial port as well as a convenient method for JTAG debugging. It eliminates the need for external chips or JTAG adapters, saving space and reducing cost.

Feature List

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- CDC-ACM virtual serial port and JTAG adapter functionality
- CDC-ACM:
  - CDC-ACM adherent serial port emulation (plug-and-play on most modern OSes)
  - Host controllable chip reset and entry into download mode
- JTAG adapter functionality:
  - Fast communication with CPU debugging core using a compact representation of JTAG instructions

- Support for reprogramming of attached flash memory through the ROM startup code
- Internal PHY

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.7 Two-wire Automotive Interface

The Two-wire Automotive Interface (TWAI®) is a multi-master, multi-cast communication protocol designed for automotive applications. The TWAI controller facilitates the communication based on this protocol.

Feature List

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- Special transmissions: Single-shot and Self Reception
- Acceptance filter (single and dual filter modes)
- Error detection and handling: error counters, configurable error warning limit, error code capture, arbitration lost capture, automatic transceiver standby

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.8 SDIO Slave Controller

The SDIO Slave Controller in the ESP32-C6 chip provides hardware support for the Secure Digital Input/Output (SDIO) device interface. It allows an SDIO host to access the ESP32-C6 via an SDIO bus protocol.

Feature List

- Compatible with SD Physical Layer Specification V2.00 and SDIO V2.00 specifications
- Support for SPI, 1-bit SDIO, and 4-bit SDIO transfer modes
- Clock range of 0 ~ 50 MHz
- Configurable sample and drive clock edge
- Integrated and SDIO-accessible registers for information interaction
- Support for SDIO interrupt mechanism
- Automatic padding data and discarding the padded data on the SDIO bus
- Block size up to 512 bytes
- Interrupt vector between the host and slave for bidirectional interrupt

- Support DMA for data transfer
- Support for wake-up from sleep when connection is retained

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.9 LED PWM Controller

The LED PWM Controller (LEDC) is designed to generate PWM signals for LED control.

Feature List

- Six independent PWM generators
- Maximum PWM duty cycle resolution of 20 bits
- Four independent timers with 20-bit counters, configurable fractional clock dividers and counter overflow values
- Adjustable phase of PWM signal output
- PWM duty cycle dithering
- Automatic duty cycle fading
  - Linear duty cycle fading — only one duty cycle range
  - Gamma curve fading — up to 16 duty cycle ranges for each PWM generator, with independently configured fading direction (increase or decrease), fading amount, number of fades, and fading frequency
- PWM signal output in low-power mode (Light-sleep mode)
- Event generation and task response achieved by the Event Task Matrix (ETM)

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.10 Motor Control PWM

The Motor Control Pulse Width Modulator (MCPWM) is designed for driving digital motors and smart light. The MCPWM is divided into five main modules: PWM timers, PWM operators, Capture module, Fault Detection module, and Event Task Matrix (ETM) module.

Feature List

- Three PWM timers for precise timing and frequency control
  - Every PWM timer has a dedicated 8-bit clock prescaler
  - The 16-bit counter in the PWM timer can work in count-up mode, count-down mode, or count-up-down mode

  - Hardware or software synchronization to trigger a reload on the PWM timer or the prescaler's restart, with selectable hardware synchronization source
- Three PWM operators for generating waveform pairs
  - Six PWM outputs to operate in several topologies
  - Configurable dead time on rising and falling edges; each set up independently
  - Modulating of PWM output by high-frequency carrier signals, useful when gate drivers are insulated with a transformer
- Capture module for hardware-based signal processing
  - Speed measurement of rotating machinery
  - Measurement of elapsed time between position sensor pulses
  - Period and duty cycle measurement of pulse train signals
  - Decoding current or voltage amplitude derived from duty-cycle-encoded signals of current/voltage sensors
  - Three individual capture channels, each of which with a 32-bit time-stamp register
  - Selection of edge polarity and prescaling of input capture signals
  - The capture timer can sync with a PWM timer or external signals
- Fault Detection module
  - Programmable fault handling in both cycle-by-cycle mode and one-shot mode
  - A fault condition can force the PWM output to either high or low logic levels
- Event generation and task response achieved by the Event Task Matrix (ETM)

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.11 Remote Control Peripheral

The Remote Control Peripheral (RMT) controls the transmission and reception of infrared remote control signals.

Feature List

- Four channels for sending and receiving infrared remote control signals
- Independent transmission and reception capabilities for each channel
- Support for Normal TX/RX mode, Wrap TX/RX mode, Continuous TX mode
- Modulation on TX pulses and Demodulation on RX pulses
- RX filtering for improved signal reception
- Ability to transmit data simultaneously on multiple channels
- Clock divider counter, state machine, and receiver for each RX channel

- Default allocation of RAM blocks to channels based on channel number
- RAM containing 16-bit entries with “level” and “period” fields

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.1.12 Parallel IO Controller

The Parallel IO Controller (PARLIO) in the ESP32-C6 chip enables data transfer between external devices and internal memory on a parallel bus through GDMA. It consists of a transmitter (TX unit) and a receiver (RX unit), making it a versatile interface for connecting various peripherals.

Feature List

- 1/2/4/8/16-bit configurable data bus width
- Half-duplex communication with 16-bit data bus width and full-duplex communication with 8-bit data bus width
- Bit reordering in 1/2/4-bit data bus width mode
- RX unit supports 15 receive modes categorized into three major categories: Level Enable mode, Pulse Enable mode, and Software Enable mode
- TX unit can generate a valid signal aligned with TX

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 SAR ADC

ESP32-C6 integrates a Successive Approximation Analog-to-Digital Converter (SAR ADC) to convert analog signals into digital representations.

Feature List

- 12-bit sampling resolution
- Analog voltage sampling from up to seven pins
- Attenuation of input signals for voltage conversion
- Software-triggered one-time sampling
- Timer-triggered multi-channel scanning
- DMA continuous conversion for seamless data transfer
- Two filters with configurable filter coefficient

- Threshold monitoring which helps to trigger an interrupt
- Support for Event Task Matrix

Pin Assignment

For details, see *ESP32-C6 Series Datasheet* > Section *Peripheral Pin Assignment*.

5.2.2.2 Temperature Sensor

The Temperature Sensor in the ESP32-C6 chip allows for real-time monitoring of temperature changes inside the chip.

Feature List

- Measurement range: −40°C ~ 125°C
- Software triggering, wherein the data can be read continuously once triggered
- Hardware automatic triggering and temperature monitoring
- Configurable temperature offset based on the environment to improve the accuracy
- Adjustable measurement range
- Two automatic monitoring wake-up modes: absolute value mode and incremental value mode
- Support for Event Task Matrix

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 6-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 6-2 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	105	°C

6.2 Recommended Operating Conditions

Table 6-2. Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	Power supply voltage		3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply		0.5	—	—	A
T_A	Operating ambient temperature	85 °C version	−40	—	85	°C
		105 °C version			105	

6.3 DC Characteristics (3.3 V, 25 °C)

Table 6-3. DC Characteristics (3.3 V, 25 °C)

Parameter	Description	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD [1]	—	VDD [1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD [1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH} [2]	High-level output voltage	0.8 × VDD [1]	—	—	V
V_{OL} [2]	Low-level output voltage	—	—	0.1 × VDD [1]	V
I_{OH}	High-level source current (VDD [1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD [1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_PU voltage is within the specified range)	0.75 × VDD [1]	—	VDD [1] + 0.3	V

V_{IL_nRST}	Chip reset voltage (CHIP_PU voltage is within the specified range)	−0.3	—	0.25 × VDD [1]	V

[1] VDD – voltage from a power pin of a respective power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4 Current Consumption Characteristics

6.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 6-4. Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @ 20.5 dBm	382
		802.11g, 54 Mbps, OFDM @ 19.0 dBm	316
		802.11n, HT20, MCS7 @ 18.0 dBm	295
		802.11n, HT40, MCS7 @ 17.5 dBm	280
		802.11ax, MCS9 @ 15.5 dBm	251
	RX	802.11b/g/n, HT20	78
		802.11n, HT40	82
		802.11ax, HE20	78

Table 6-5. Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 19.0 dBm	309
		Bluetooth LE @ 9.0 dBm	190
		Bluetooth LE @ 0 dBm	130
		Bluetooth LE @ −16.0 dBm	93
	RX	Bluetooth LE	73

Table 6-6. Current Consumption for 802.15.4 in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.15.4 @ 19.0 dBm	302
		802.15.4 @ 12.0 dBm	185
		802.15.4 @ 0 dBm	117
		802.15.4 @ −16.0 dBm	91
	RX	802.15.4	73

Note:
The content below is excerpted from *Section Current Consumption in Other Modes* in *ESP32-C6 Series Datasheet*.

6.4.2 Current Consumption in Other Modes

Table 6-7. Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled [1]
Modem-sleep [2, 3]	160	CPU is running	27	38
		CPU is idle	17	28
	80	CPU is running	19	30
		CPU is idle	14	25

[1] In practice, the current consumption might be different depending on which peripherals are enabled.
[2] In Modem-sleep mode, Wi-Fi is clock gated.
[3] In Modem-sleep mode, the consumption might be higher when accessing flash.

Table 6-8. Current Consumption in Low-Power Modes

Mode	Description	Typ (μA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	180
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	35
Deep-sleep	RTC timer and LP memory are powered on	7
Power off	CHIP_PU is set to low level, the chip is powered off	1

6.5 Memory Specifications

The data below is sourced from the memory vendor datasheet. These values are guaranteed through design and/or characterization but are not fully tested in production. Devices are shipped with the memory erased.

Table 6-9. Flash Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.65	1.80	2.00	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz
—	Program/erase cycles	100,000	—	—	cycles
T_{RET}	Data retention time	20	—	—	years
T_{PP}	Page program time	—	0.8	5	ms

Cont'd on next page

Table 6-9 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
T_{SE}	Sector erase time (4 KB)	—	70	500	ms
T_{BE1}	Block erase time (32 KB)	—	0.2	2	s
T_{BE2}	Block erase time (64 KB)	—	0.3	3	s
T_{CE}	Chip erase time (16 Mb)	—	7	20	s
	Chip erase time (32 Mb)	—	20	60	s
	Chip erase time (64 Mb)	—	25	100	s
	Chip erase time (128 Mb)	—	60	200	s
	Chip erase time (256 Mb)	—	70	300	s

7 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

7.1 Wi-Fi Radio

Table 7-1. Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n/ax

7.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 7-2. TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	20.5	—
802.11b, 11 Mbps, CCK	—	20.5	—
802.11g, 6 Mbps, OFDM	—	20.0	—
802.11g, 54 Mbps, OFDM	—	19.0	—
802.11n, HT20, MCS0	—	19.0	—
802.11n, HT20, MCS7	—	18.0	—
802.11n, HT40, MCS0	—	18.5	—
802.11n, HT40, MCS7	—	17.5	—
802.11ax, HE20, MCS0	—	19.0	—
802.11ax, HE20, MCS9	—	15.5	—

Table 7-3. TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–25.0	–10.0
802.11b, 11 Mbps, CCK	—	–25.0	–10.0

Cont'd on next page

Table 7-3 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11g, 6 Mbps, OFDM	—	–24.0	–5.0
802.11g, 54 Mbps, OFDM	—	–28.0	–25.0
802.11n, HT20, MCS0	—	–27.5	–5.0
802.11n, HT20, MCS7	—	–30.0	–27.0
802.11n, HT40, MCS0	—	–27.0	–5.0
802.11n, HT40, MCS7	—	–29.5	–27.0
802.11ax, HE20, MCS0	—	–27.0	–5.0
802.11ax, HE20, MCS9	—	–34.0	–32.0

[1] EVM is measured at the corresponding typical TX power provided in Table *7-2 TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

7.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n/ax.

Table 7-4. RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–99.2	—
802.11b, 2 Mbps, DSSS	—	–96.8	—
802.11b, 5.5 Mbps, CCK	—	–93.6	—
802.11b, 11 Mbps, CCK	—	–90.0	—
802.11g, 6 Mbps, OFDM	—	–94.0	—
802.11g, 9 Mbps, OFDM	—	–93.0	—
802.11g, 12 Mbps, OFDM	—	–92.4	—
802.11g, 18 Mbps, OFDM	—	–90.0	—
802.11g, 24 Mbps, OFDM	—	–86.8	—
802.11g, 36 Mbps, OFDM	—	–83.0	—
802.11g, 48 Mbps, OFDM	—	–78.8	—
802.11g, 54 Mbps, OFDM	—	–77.6	—
802.11n, HT20, MCS0	—	–93.6	—
802.11n, HT20, MCS1	—	–92.0	—
802.11n, HT20, MCS2	—	–89.4	—
802.11n, HT20, MCS3	—	–86.0	—
802.11n, HT20, MCS4	—	–82.8	—
802.11n, HT20, MCS5	—	–78.6	—
802.11n, HT20, MCS6	—	–77.0	—
802.11n, HT20, MCS7	—	–75.4	—
802.11n, HT40, MCS0	—	–91.0	—
802.11n, HT40, MCS1	—	–89.6	—

Cont'd on next page

Table 7-4 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS2	—	–87.0	—
802.11n, HT40, MCS3	—	–83.4	—
802.11n, HT40, MCS4	—	–80.4	—
802.11n, HT40, MCS5	—	–76.2	—
802.11n, HT40, MCS6	—	–74.6	—
802.11n, HT40, MCS7	—	–73.2	—
802.11ax, HE20, MCS0	—	–93.8	—
802.11ax, HE20, MCS1	—	–91.0	—
802.11ax, HE20, MCS2	—	–88.0	—
802.11ax, HE20, MCS3	—	–85.6	—
802.11ax, HE20, MCS4	—	–82.0	—
802.11ax, HE20, MCS5	—	–78.0	—
802.11ax, HE20, MCS6	—	–76.6	—
802.11ax, HE20, MCS7	—	–74.4	—
802.11ax, HE20, MCS8	—	–70.8	—
802.11ax, HE20, MCS9	—	–68.6	—

Table 7-5. Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—
802.11ax, HE20, MCS0	—	5	—
802.11ax, HE20, MCS9	—	0	—

Table 7-6. RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	38	—
802.11b, 11 Mbps, CCK	—	38	—
802.11g, 6 Mbps, OFDM	—	31	—
802.11g, 54 Mbps, OFDM	—	20	—

Cont'd on next page

Table 7-6 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	16	—
802.11n, HT40, MCS0	—	28	—
802.11n, HT40, MCS7	—	10	—
802.11ax, HE20, MCS0	—	25	—
802.11ax, HE20, MCS9	—	2	—

7.2 Bluetooth 5 (LE) Radio

Table 7-7. Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–16.0 ~ 19.0 dBm

7.2.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 7-8. Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	1.3	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.5	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	0.9	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.6	—	kHz
Modulation characteristics	$\Delta\, F1_{avg}$	—	249.9	—	kHz
	Min. $\Delta\, F2_{max}$ (for at least 99.9% of all $\Delta\, F2_{max}$)	—	212.1	—	kHz
	$\Delta\, F2_{avg} / \Delta\, F1_{avg}$	—	0.88	—	—
In-band emissions	± 2 MHz offset	—	–29	—	dBm
	± 3 MHz offset	—	–36	—	dBm
	> ± 3 MHz offset	—	–39	—	dBm

Table 7-9. Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	2.2	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	1.1	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.1	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.5	—	kHz
Modulation characteristics	$\Delta\, F1_{avg}$	—	499.4	—	kHz

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Table 7-9 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	443.5	–	kHz
	$\Delta F2_{avg}/\Delta F1_{avg}$	–	0.95	–	–
In-band emissions	± 4 MHz offset	–	–40	–	dBm
	± 5 MHz offset	–	–41	–	dBm
	> ± 5 MHz offset	–	–42	–	dBm

Table 7-10. Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	0.7	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	0.3	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.1	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	0.4	–	kHz
Modulation characteristics	$\Delta F1_{avg}$	–	250.0	–	kHz
	Min. $\Delta F1_{max}$ (for at least 99.9% of all $\Delta F1_{max}$)	–	238.0	–	kHz
In-band emissions	± 2 MHz offset	–	–29	–	dBm
	± 3 MHz offset	–	–36	–	dBm
	> ± 3 MHz offset	–	–39	–	dBm

Table 7-11. Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	–	0.5	–	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	–	0.3	–	kHz
	$\lvert f_0 - f_3 \rvert$	–	0.1	–	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	–	0.4	–	kHz
Modulation characteristics	$\Delta F2_{avg}$	–	230.7	–	kHz
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	–	217.6	–	kHz
In-band emissions	± 2 MHz offset	–	–28	–	dBm
	± 3 MHz offset	–	–36	–	dBm
	> ± 3 MHz offset	–	–39	–	dBm

7.2.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 7-12. Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	–	–	–98.0	–	dBm
Maximum received signal @30.8% PER	–	–	8	–	dBm

Cont'd on next page

Table 7-12 – cont'd from previous page

Parameter		Description	Min	Typ	Max	Unit
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	7	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	4	—	dB
		F = F0 – 1 MHz	—	3	—	dB
		F = F0 + 2 MHz	—	–21	—	dB
		F = F0 – 2 MHz	—	–22	—	dB
		F = F0 + 3 MHz	—	–28	—	dB
		F = F0 – 3 MHz	—	–36	—	dB
		F ≥ F0 + 4 MHz	—	–27	—	dB
		F ≤ F0 – 4 MHz	—	–36	—	dB
	Image frequency	—	—	–26	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–29	—	dB
		F = F_{image} – 1 MHz	—	–28	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–16	—	dBm
		2003 MHz ~ 2399 MHz	—	–24	—	dBm
		2484 MHz ~ 2997 MHz	—	–16	—	dBm
		3000 MHz ~ 12.75 GHz	—	–1	—	dBm
Intermodulation		—	—	–27	—	dBm

Table 7-13. Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–95.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	8	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	3	—	dB
		F = F0 – 2 MHz	—	2	—	dB
		F = F0 + 4 MHz	—	–23	—	dB
		F = F0 – 4 MHz	—	–25	—	dB
		F = F0 + 6 MHz	—	–31	—	dB
		F = F0 – 6 MHz	—	–35	—	dB
		F ≥ F0 + 8 MHz	—	–36	—	dB
		F ≤ F0 – 8 MHz	—	–36	—	dB
	Image frequency	—	—	–23	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–30	—	dB
		F = F_{image} – 2 MHz	—	3	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–18	—	dBm
		2003 MHz ~ 2399 MHz	—	–28	—	dBm
		2484 MHz ~ 2997 MHz	—	–16	—	dBm
		3000 MHz ~ 12.75 GHz	—	–1	—	dBm
Intermodulation		—	—	–29	—	dBm

Table 7-14. Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–105.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	2	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–1	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–31	—	dB
		F = F0 – 2 MHz	—	–27	—	dB
		F = F0 + 3 MHz	—	–33	—	dB
		F = F0 – 3 MHz	—	–42	—	dB
		F ≥ F0 + 4 MHz	—	–31	—	dB
		F ≤ F0 – 4 MHz	—	–48	—	dB
	Image frequency	—	—	–31	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–33	—	dB

Table 7-15. Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–101.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	1	—	dB
		F = F0 – 1 MHz	—	–1	—	dB
		F = F0 + 2 MHz	—	–23	—	dB
		F = F0 – 2 MHz	—	–24	—	dB
		F = F0 + 3 MHz	—	–33	—	dB
		F = F0 – 3 MHz	—	–41	—	dB
		F ≥ F0 + 4 MHz	—	–31	—	dB
		F ≤ F0 – 4 MHz	—	–41	—	dB
	Image frequency	—	—	–30	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–35	—	dB
		F = F_{image} – 1 MHz	—	–27	—	dB

7.3 802.15.4 Radio

Table 7-16. 802.15.4 RF Characteristics

Name	Description
Center frequency range of operating channel	2405 ~ 2480 MHz

[1] Zigbee in the 2.4 GHz range supports 16 channels at 5 MHz spacing from channel 11 to channel 26.

7.3.1 802.15.4 RF Transmitter (TX) Characteristics

Table 7-17. 802.15.4 Transmitter Characteristics - 250 Kbps

Parameter	Min	Typ	Max	Unit
RF transmit power range	–16.0	—	19.0	dBm
EVM	—	13%	—	—

7.3.2 802.15.4 RF Receiver (RX) Characteristics

Table 7-18. 802.15.4 Receiver Characteristics - 250 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @1% PER		—	—	–104.0	—	dBm
Maximum received signal @1% PER		—	—	8	—	dBm
Relative jamming level	Adjacent channel	F = F0 + 5 MHz	—	27	—	dB
		F = F0 – 5 MHz	—	32	—	dB
	Alternate channel	F = F0 + 10 MHz	—	47	—	dB
		F = F0 – 10 MHz	—	50	—	dB

8 Module Schematics

This is the reference design of the module.

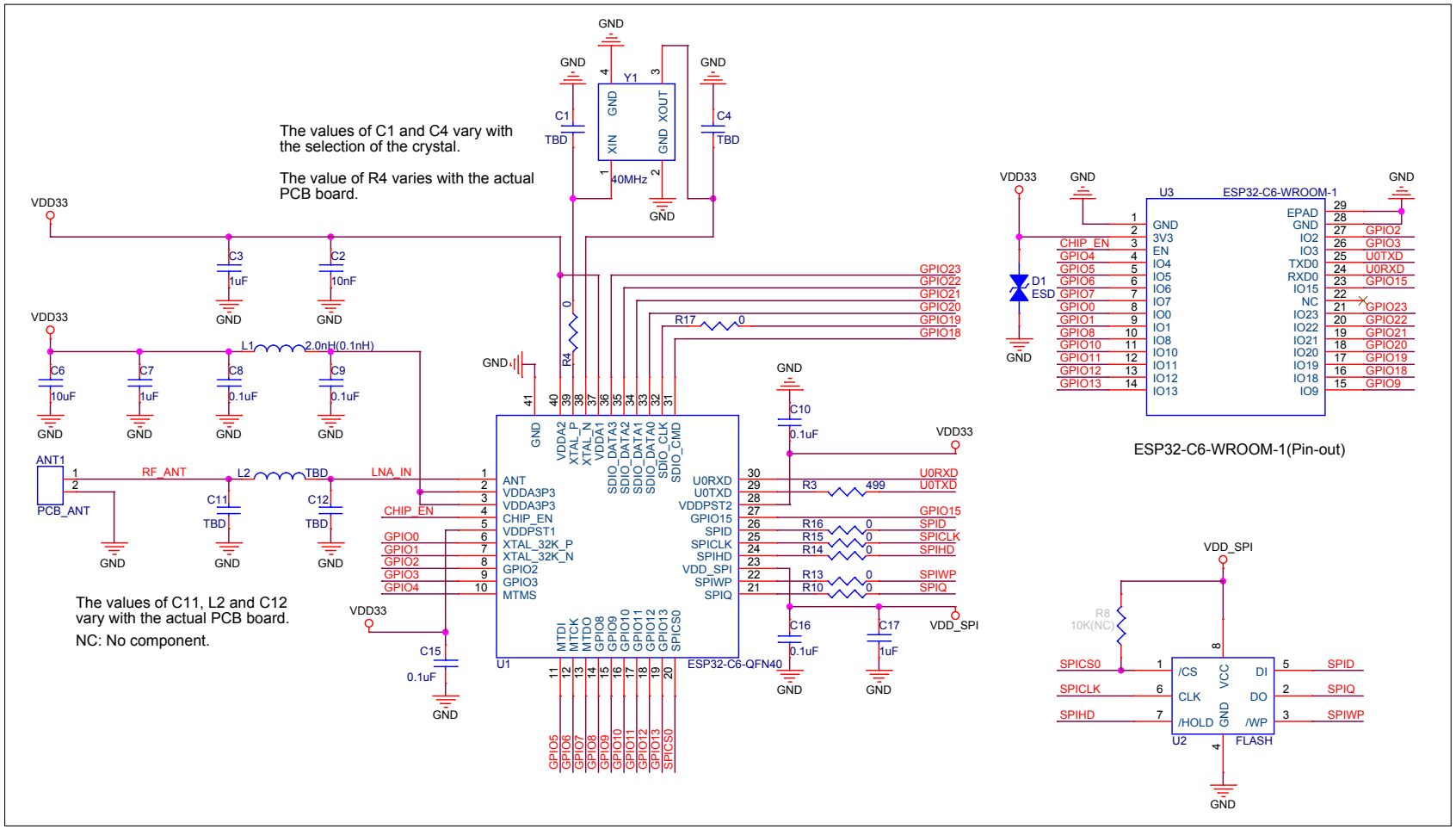


Figure 8-1. ESP32-C6-WROOM-1 Schematics

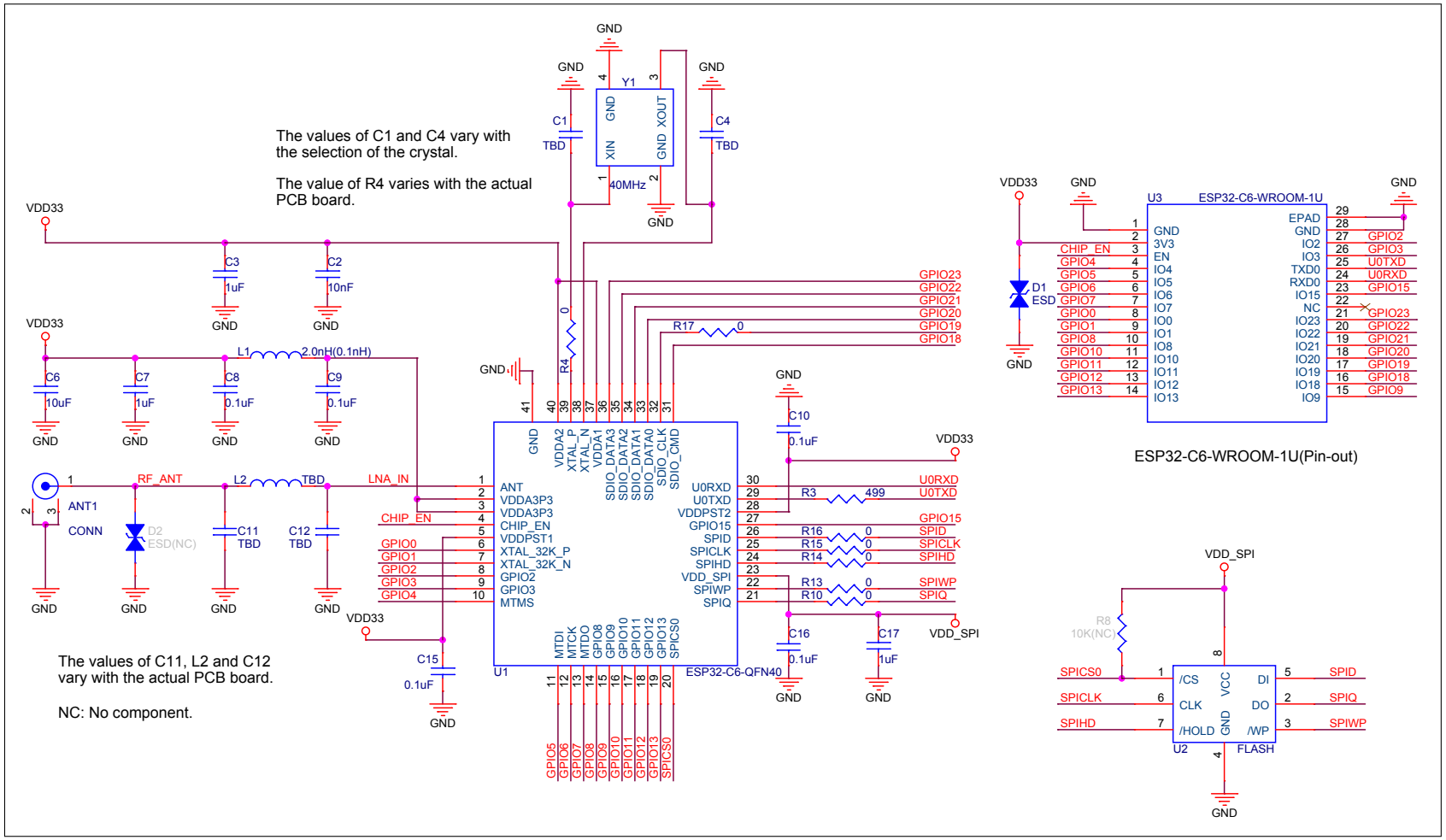


Figure 8-2. ESP32-C6-WROOM-1U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

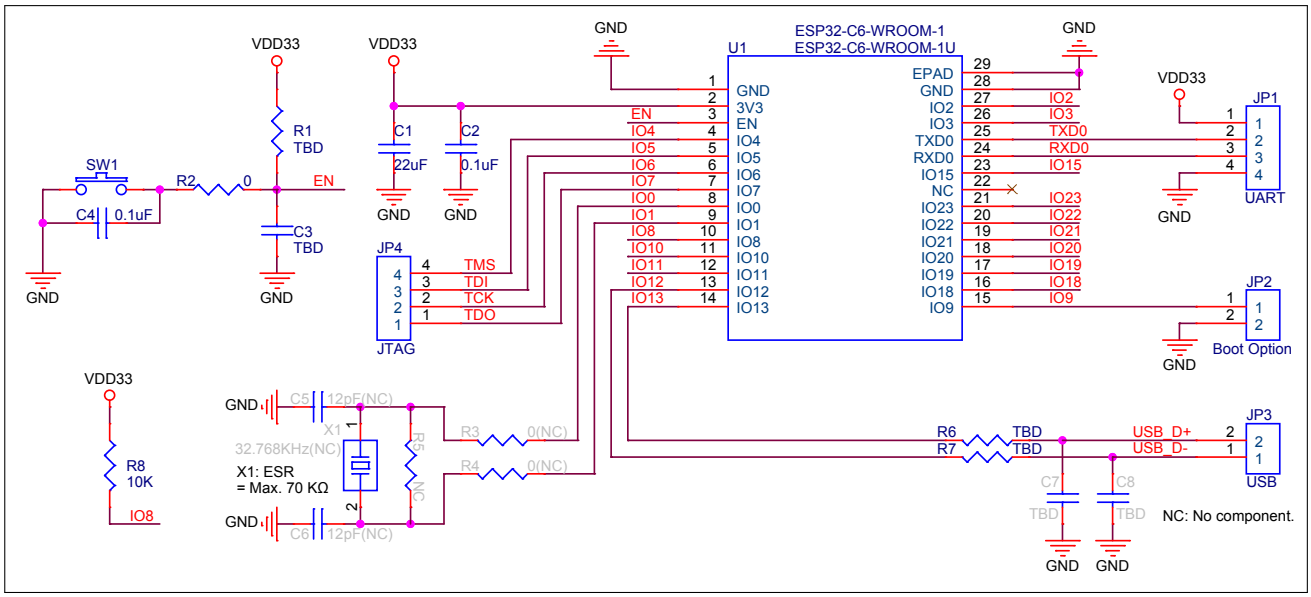


Figure 9-1. Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-C6 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-C6's power-up and reset sequence timing diagram, please refer Section 4.5 *Chip Power-up and Reset*.

10 Physical Dimensions

10.1 Physical Dimensions

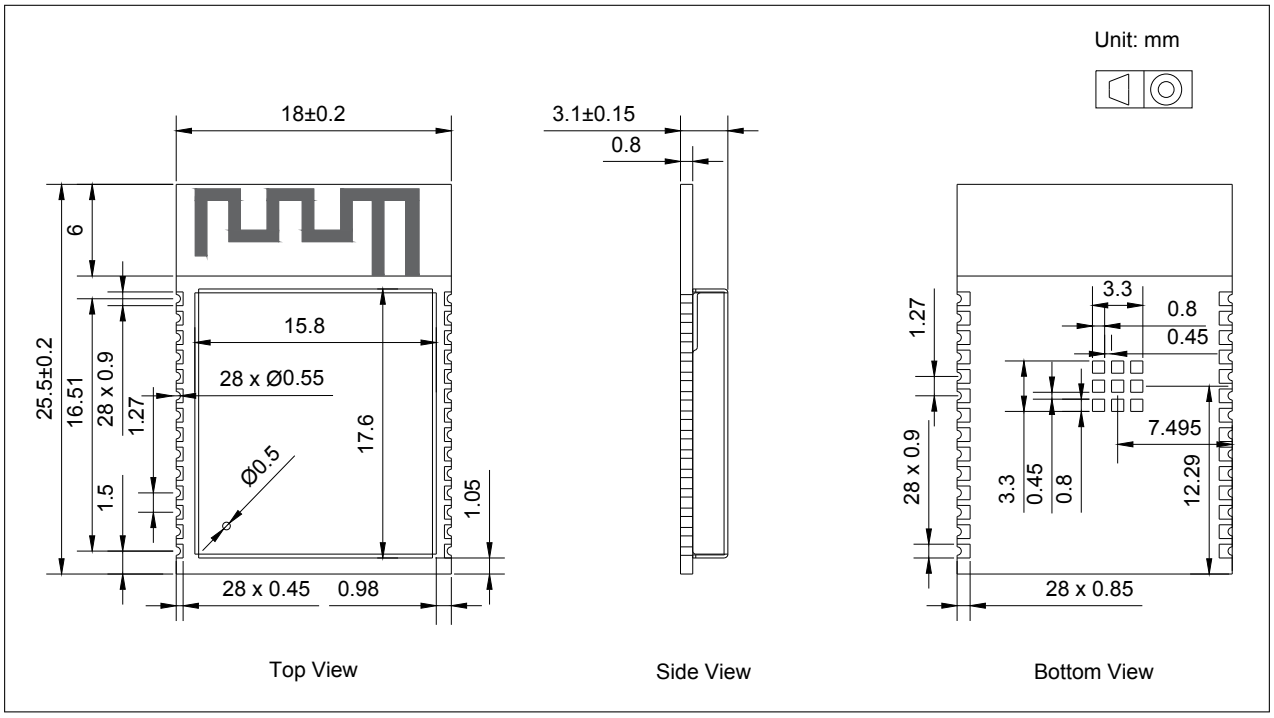


Figure 10-1. ESP32-C6-WROOM-1 Physical Dimensions

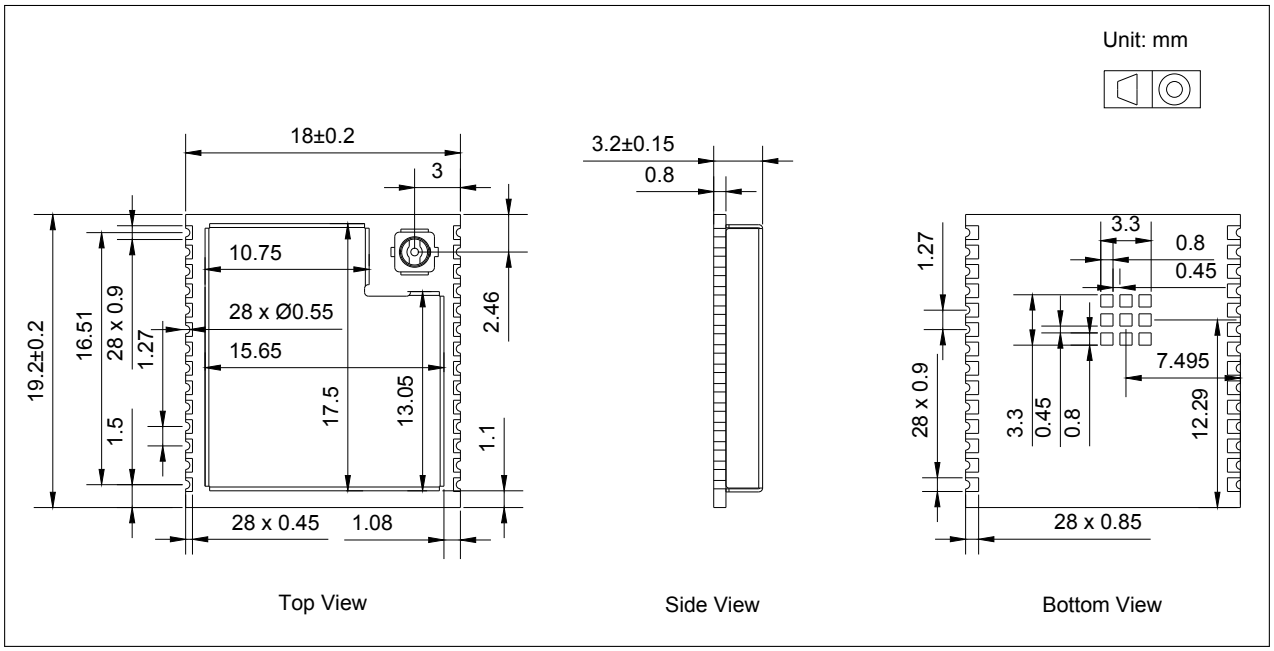


Figure 10-2. ESP32-C6-WROOM-1U Physical Dimensions

Note:
For information about tape, reel, and product marking, please refer to *ESP32-C6 Module Packaging Information*.

10.2 Dimensions of External Antenna Connector

ESP32-C6-WROOM-1U uses the first generation external antenna connector as shown in Figure 10-3 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

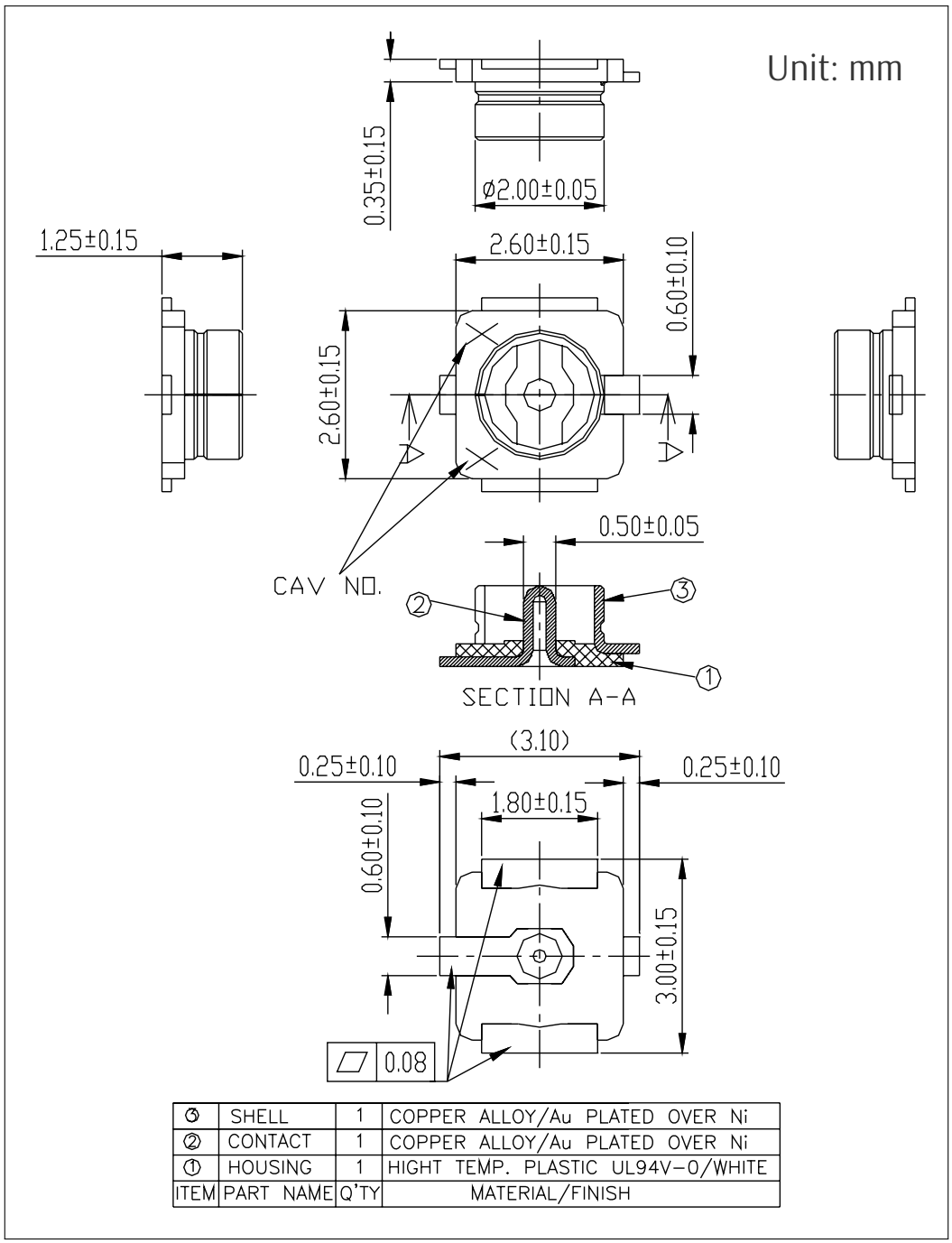


Figure 10-3. Dimensions of External Antenna Connector

The external antenna used for ESP32-C6-WROOM-1U during certification testing is the first generation monopole antenna, with material code TFPD05H08750011.

The module does not include an external antenna upon shipment. If needed, select a suitable external antenna based on the product's usage environment and performance requirements.

It is recommended to select an antenna that meets the following requirements:

- 2.4 GHz band
- 50 Ω impedance
- The maximum gain does not exceed 2.33 dBi, the gain of the antenna used for certification
- The connector matches the specifications shown in Figure 10-3 *Dimensions of External Antenna Connector*

Note:
If you use an external antenna of a different type or gain, additional testing, such as EMC, may be required beyond the existing antenna test reports for Espressif modules. Specific requirements depend on the certification type.

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 11-1 *ESP32-C6-WROOM-1 Recommended PCB Land Pattern* and Figure 11-2 *ESP32-C6-WROOM-1U Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 11-1 and Figure 11-2. You can view the source files for ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U with Autodesk Viewer.
- 3D models of ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

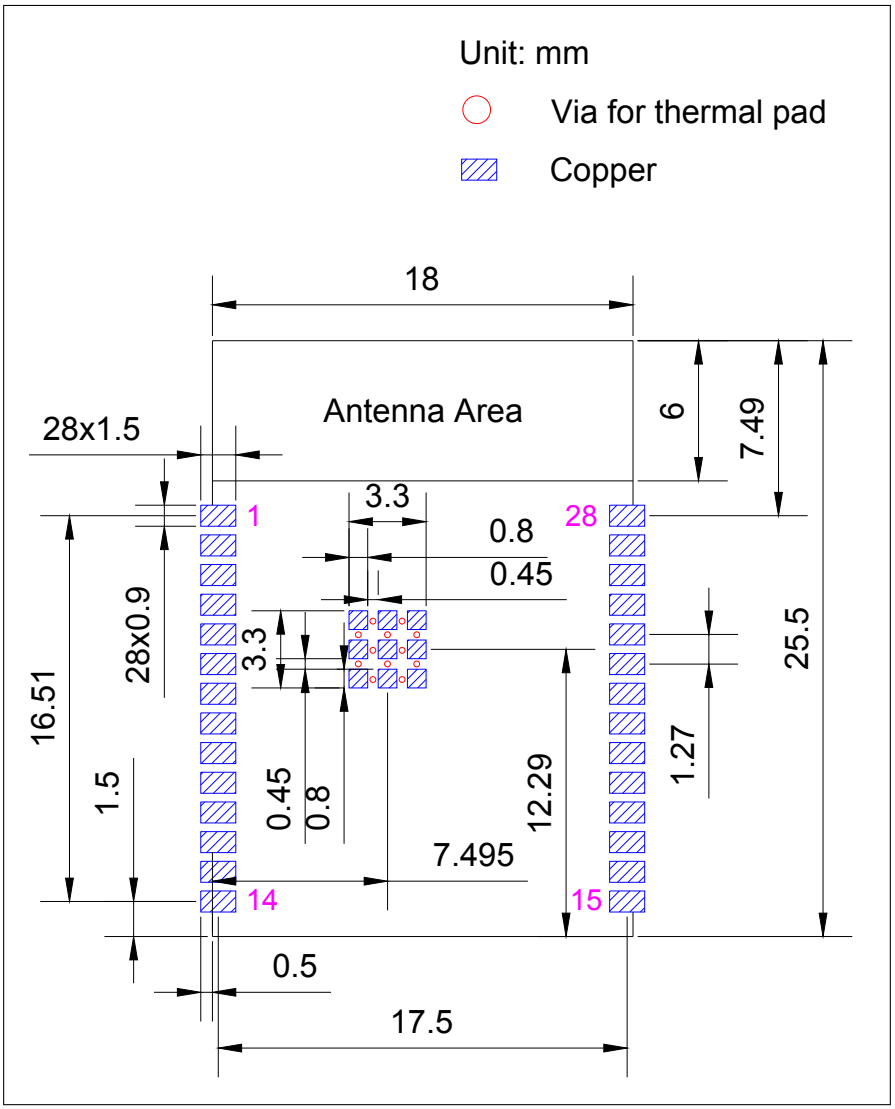


Figure 11-1. ESP32-C6-WROOM-1 Recommended PCB Land Pattern

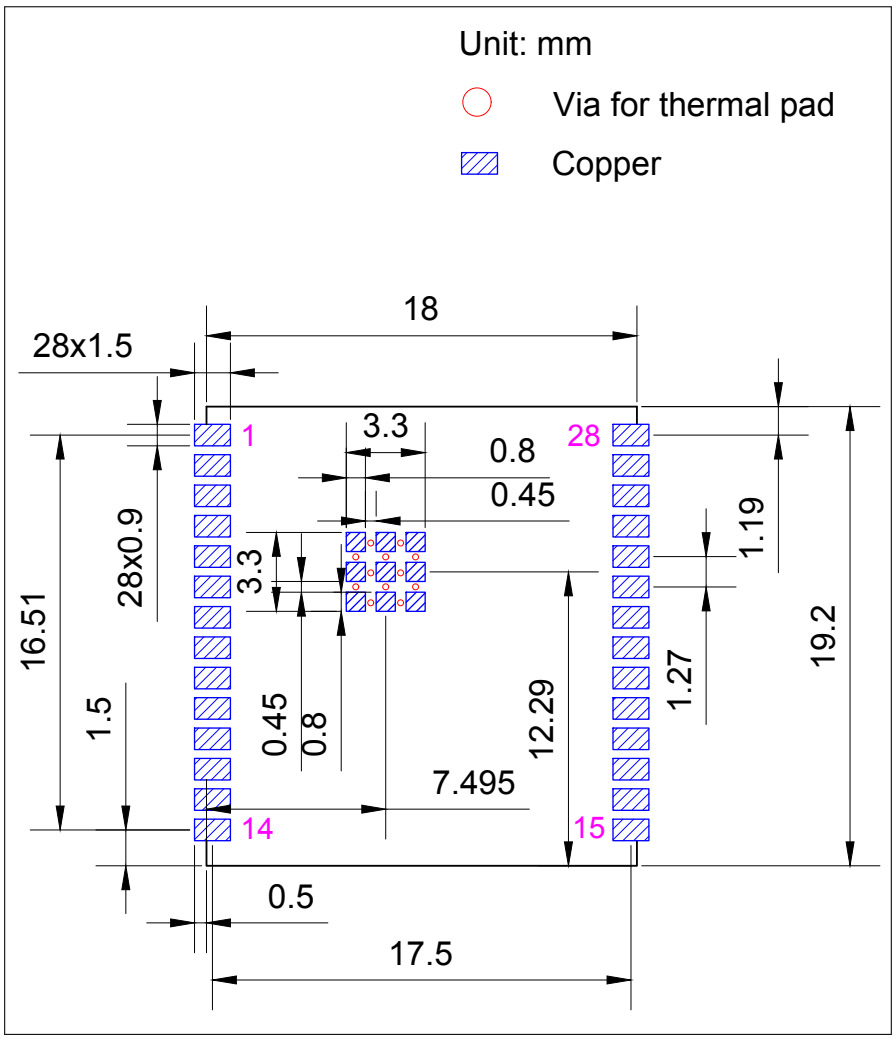


Figure 11-2. ESP32-C6-WROOM-1U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-C6 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12 Product Handling

12.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

12.3 Reflow Profile

Solder the module in a single reflow.

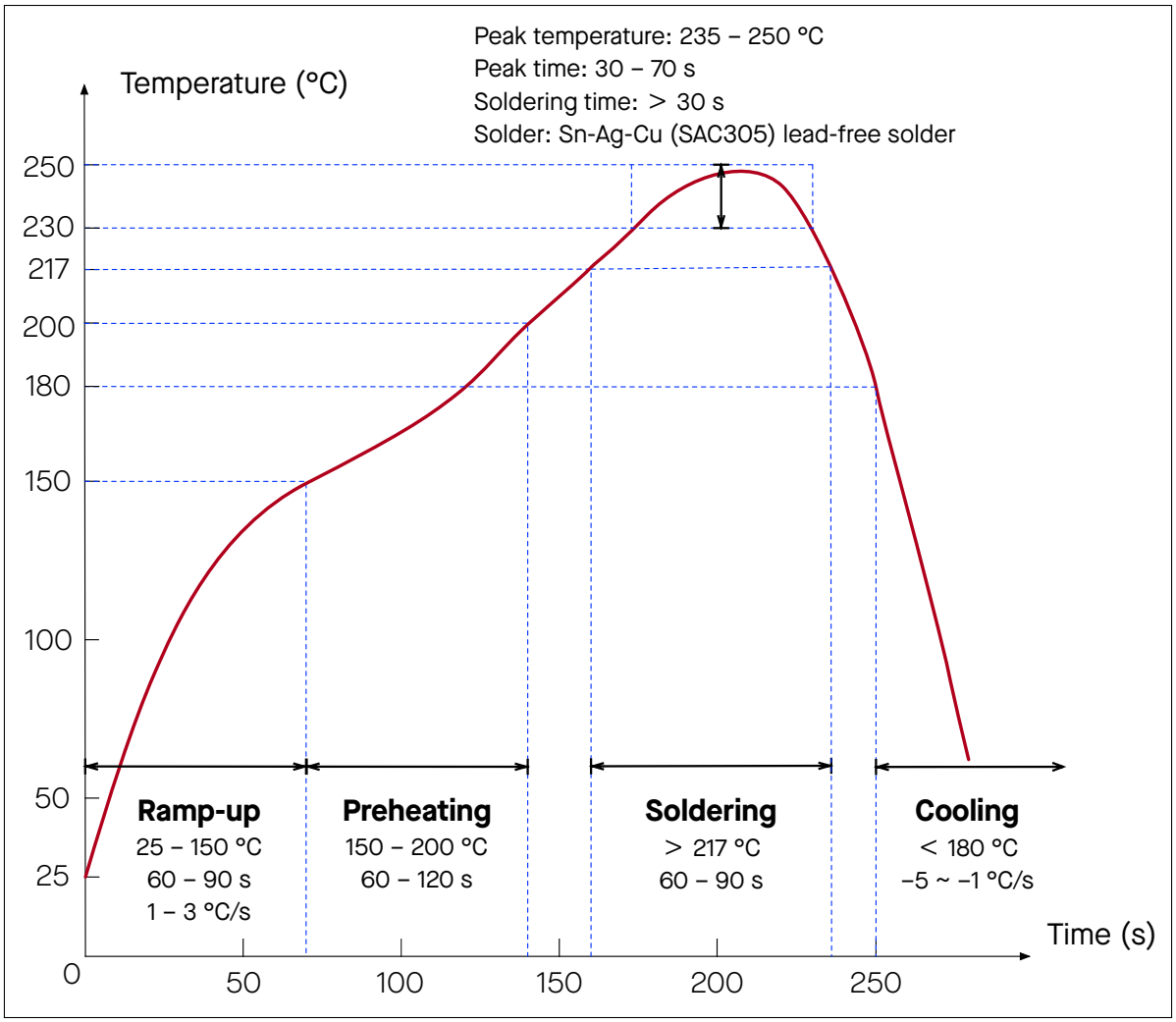


Figure 12-1. Reflow Profile

12.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Datasheet Versioning

Datasheet Version	Status	Watermark	Definition
v0.1 ~ v0.5 (excluding v0.5)	Draft	Confidential	This datasheet is under development for products in the design stage. Specifications may change without prior notice.
v0.5 ~ v1.0 (excluding v1.0)	Preliminary release	Preliminary	This datasheet is actively updated for products in the verification stage. Specifications may change before mass production, and the changes will be documentation in the datasheet's Revision History.
v1.0 and higher	Official release	—	This datasheet is publicly released for products in mass production. Specifications are finalized, and major changes will be communicated via Product Change Notifications (PCN).
Any version	—	Not Recommended for New Design (NRND)[1]	This datasheet is updated less frequently for products not recommended for new designs.
Any version	—	End of Life (EOL)[2]	This datasheet is no longer mtained for products that have reached end of life.

[1] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet are not recommended for new designs.

[2] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet have reached end of life.

Related Documentation and Resources

Related Documentation

- ESP32-C6 Series Datasheet – Specifications of the ESP32-C6 hardware.
- ESP32-C6 Technical Reference Manual – Detailed information on how to use the ESP32-C6 memory and peripherals.
- ESP32-C6 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-C6 into your hardware product.
- ESP32-C6 Series SoC Errata – Descriptions of known errors in ESP32-C6 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-C6 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C6
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-C6 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *ESP-FAQ* – A summary document of frequently asked questions released by Espressif.
  https://espressif.com/projects/esp-faq/en/latest/index.html
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C6 Series SoCs* – Browse through all ESP32-C6 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C6
- *ESP32-C6 Series Modules* – Browse through all ESP32-C6-based modules.
  https://espressif.com/en/products/modules?id=ESP32-C6
- *ESP32-C6 Series DevKits* – Browse through all ESP32-C6-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-C6
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2025-12-10	v1.4	In Section 1.2 *Series Comparison*: • Updated "Ordering Code" to "Part Number" • Added information about ESP32-C6-WROOM-1-N16 and ESP32-C6-WROOM-1U-N16
2025-07-17	v1.3	• In Chapter 2 *Block Diagram*, added a note about pin mapping between the chip and the in-package flash • In Chapter 10.2 *Dimensions of External Antenna Connector*, added the external antenna information for certification • Added Sections 4.5 *Chip Power-up and Reset*, 6.5 *Memory Specifications* and *Datasheet Versioning*
2025-03-21	v1.2	• In Chapter 1 *Module Overview*, renamed Section 1.2 *Description* to 1.2 *Series Comparison*, and added a table note about the maximum clock frequency supported by SPI flash • In Table 6-1 *Absolute Maximum Ratings* of Section 6 *Electrical Characteristics*, updated the maximum storage temperature from 85°C to 105°C • Improved the structure, formatting, and wording in: – Chapter 4 *Boot Configurations* (used to be Section 3.3 *Strapping Pins*) – Chapter 5 *Peripherals* (used to be Chapter 4 *Peripherals*) – Chapter 10 *Physical Dimensions* and Chapter 11 *PCB Layout Recommendations* (used to be Chapter 9 *Physical Dimensions and PCB Land Pattern*) • Added Section 11.2 *Module Placement for PCB Design*
2024-01-19	v1.1	• In Section 1.1 *Features*, added information about certification and test • In Section 1.2 *Series Comparison*, the minimum RF transmit power for Bluetooth LE and 802.15.4 in active mode was updated from -24 dBm to -16 dBm, and the maximum power was updated from 20 dBm to 19 dBm • In Chapter 7 *RF Characteristics*, the RF transmit power range for Bluetooth LE and 802.15.4 was updated from -24 ~ 20 dBm to -16 ~ 19 dBm • In Section 11 *PCB Layout Recommendations*, added information about the recommended PCB land pattern of ESP32-C6-WROOM-1U module, and 3D models of ESP32-C6-WROOM-1 and ESP32-C6-WROOM-1U modules

Cont'd on next page

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Date	Version	Release notes
2023-07-04	v1.0	• Updated the vector picture of ESP32-C6-WROOM-1U on the titlepage to remove the castellated pins at the bottom • In Section 1.2 *Series Comparison*, removed peripheral-related information and information on ESP32-C6-WROOM-1-H4, ESP32-C6-WROOM-1-N16, ESP32-C6-WROOM-1U-H4, and ESP32-C6-WROOM-1U-N16, and added a note about module customization • Added Chapter 5 *Peripherals* • Updated Figure 10-1 *ESP32-C6-WROOM-1 Physical Dimensions* and Figure 10-2 *ESP32-C6-WROOM-1U Physical Dimensions* to change the tolerance in the top view from 0.25 to 0.2
2023-04-17	v0.6	Added information about ESP32-C6-WROOM-1U module
2023-02-16	v0.5	Preliminary release



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G5LE
PCB Power Relay

Cubic, Single-pole 10A Power Relay



- Ideal for a wide variety of applications such as home appliances, OA equipments, vending machines, etc.
- Ambient Operating Temperature 85°C
- UL class-B coil insulation for standard model.
- UL, CSA, EN standards approved and conforms to Electrical Appliance and Material Safety Law (300 V max.).

RoHS Compliant

■Model Number Legend

G5LE-□□□-□-□
1 2 3 4 5

1. **Number of Poles**
   1: 1-pole
2. **Contact Form**
   None: SPDT (1c)
   A: SPST-NO (1a)
3. **Enclosure rating**
   None: Flux protection
   4: Fully sealed
4. **Insulation System**
   None: Class B (Class F for -E versions)
   CF: Class F (UL and CSA only)
5. **Approved Standards**
   None: Standard
   E: High capacity type

■Application Examples

- Home appliances
- OA equipments
- Vending machines

■Ordering Information

Terminal Shape	Classification	Enclosure rating / Contact form	Flux protection Model	Flux protection Rated coil voltage	Fully sealed Model	Fully sealed Rated coil voltage	Minimun packing unit
PCB terminals	Standard	SPDT (1c)	**G5LE-1**	5 VDC	**G5LE-14**	5 VDC	100 pcs/tray
				12 VDC		12 VDC	
				24 VDC		24 VDC	
			G5LE-1-CF	5 VDC	**G5LE-14-CF**	5 VDC	
				12 VDC		12 VDC	
				24 VDC		24 VDC	
		SPST-NO (1a)	**G5LE-1A**	5 VDC	**G5LE-1A4**	5 VDC	
				12 VDC		12 VDC	
				24 VDC		24 VDC	
			G5LE-1A-CF	5 VDC	**G5LE-1A4-CF**	5 VDC	
				12 VDC		12 VDC	
				24 VDC		24 VDC	
	High capacity	SPDT (1c)	**G5LE-1-E**	5 VDC	---		
				12 VDC			
				24 VDC			
		SPST-NO (1a)	**G5LE-1A-E**	5 VDC	---		
				12 VDC			
				24 VDC			

Note. When ordering, add the rated coil voltage to the model number.
Example: G5LE-1 DC5
Rated coil voltage

However, the notation of the coil voltage on the product case as well as on the packing will be marked as □□ VDC.

■Ratings

Item \ Classification / Load	Standard type Resistive load	Standard type Inductive load (cosϕ=0.4)	High capacity type Resistive load
Contact type	Single		
Contact material	Ag-alloy (Cd free)		
Rated load	10 A at 120 VAC, 8 A at 30 VDC	5 A at 120 VAC, 4 A at 30 VDC	16 A at 250 VAC (NO) 12 A at 250 VAC (NC)
Rated carry current	10 A		16A (NO)/12A (NC)
Max. switching voltage	250 VAC, 125 VDC (30 VDC when UL/CSA standard is applied)		250 VAC
Max. switching current	10 A	5 A	16A (NO)/12A (NC)

■Characteristics

Item	Classification	Standard type	High capacity type
Contact resistance *1		100 mΩ max.	
Operate time		10 ms max.	
Release time		5 ms max.	
Insulation resistance *2		100 MΩ min.	
Dielectric strength	Between coil and contacts	2,000 VAC, 50/60 Hz for 1 min	
	Between contacts of the same polarity	750 VAC, 50/60 Hz for 1 min	
Impulse withstand voltage	between coil and contacts	4,500 V (1.2×50 μs)	
Vibration resistance	Destruction	10 to 55 to 10 Hz, 0.75 mm single amplitude (1.5 mm double amplitude)	
	Malfunction	10 to 55 to 10 Hz, 0.75 mm single amplitude (1.5 mm double amplitude)	
Shock resistance	Destruction	1,000 m/s²	
	Malfunction	100 m/s²	
Durability	Mechanical	10,000,000 operations min. (at 18,000 operations/hr)	
	Electrical	100,000 operations min. (at 1,800 operations/hr)	50,000 operations min. (NO) 30,000 operations min. (NC) (at 1,800 operations/hr)
Failure rate (P level) (reference value) *3		100 mA at 5 VDC	
Ambient operating temperature		-25°C to 85°C (with no icing or condensation)	
Ambient operating humidity		35% to 85%	
Weight		Approx. 12 g	

Note. The data given above are initial values

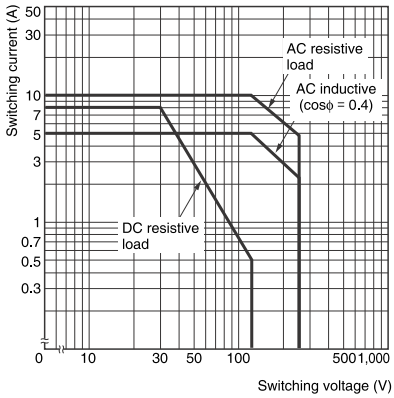
*1. Measurement conditions: 5 VDC, 1 A, voltage drop method.

*2. Measurement conditions: The insulation resistance was measured with a 500 VDC megohmmeter at the same locations as the dielectric strength was measured.

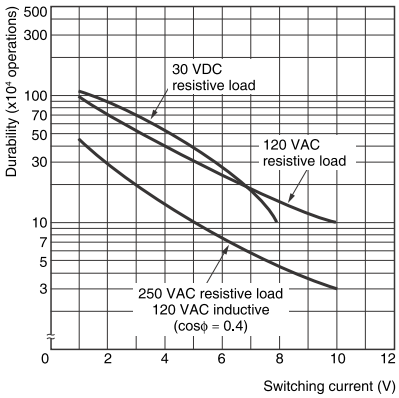
*3. This value was measured at a switching frequency of 120 operations/min.

■Engineering Data

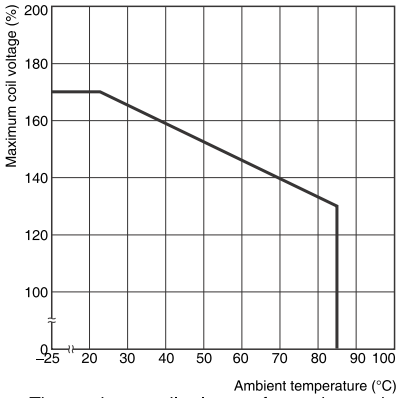
●Maximum Switching Capacity



●Durability

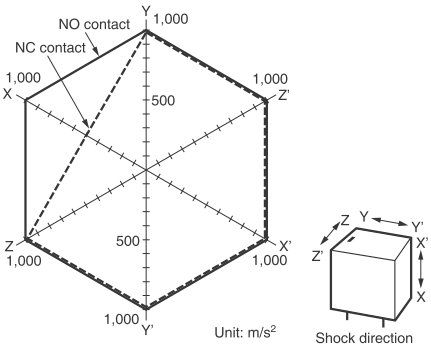


●Ambient Temperature vs. Maximum Coil Voltage



Note. The maximum coil voltage refers to the maximum value in a varying range of operating power voltage, not a continuous voltage.

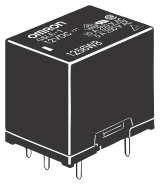
●Shock Malfunction

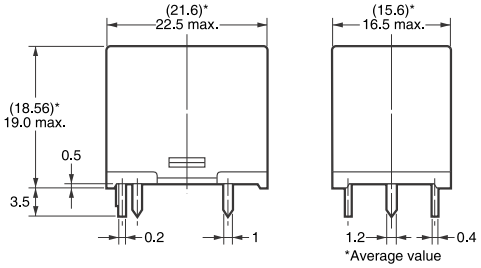


Number of Relays:5 pcs
Test Conditions: Shock was applied 3 times in each direction with and without excitation and the level at which the shock caused malfunction was measured.
Rating: 100 m/s²

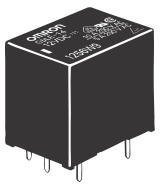
■Dimensions

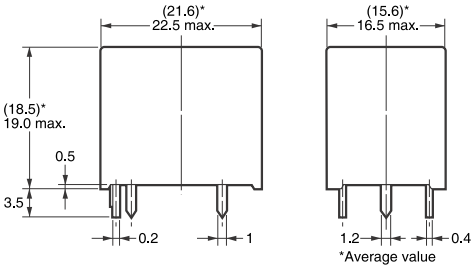
G5LE-1 (-□) (SPDT contact)
G5LE-1A (-□) (SPST-NO contact)





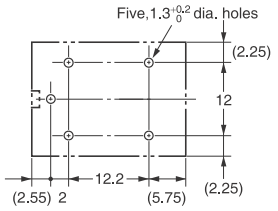
G5LE-14 (-□) (SPDT contact)
G5LE-1A4 (-□) (SPST-NO contact)





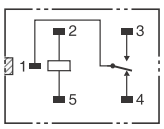
PCB Mounting Holes
(Bottom View)
Tolerance: ±0.1 mm unless specified

SPDT (1c)



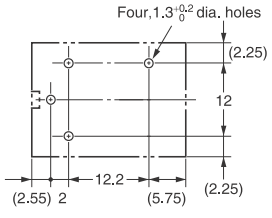
Terminal Arrangement/ Internal Connections
(Bottom View)

SPDT (1c)

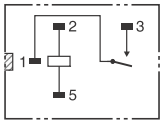


(Indicates average dimensions.)

SPST-NO (1a)



SPST-NO (1a)



(Indicates average dimensions.)

Note. Orientation marks are indicated as follows: ⬚ ▨

■Approved Standards

UL Recognized: (File No. E41643)

Model	Contact form	Coil ratings	Contact ratings	Number of test operations
G5LE	SPDT-NO (1a) SPDT (1c)	5 to 24 VDC	10 A, 250 VAC (general use) at 40°C	6,000
			8 A, 30 VDC (resistive load) at 40°C	
			TV-3 (N.O only) at 40°C	25,000
G5LE-E			13 A, 120 VAC, (resistive load) (NO only) at 85°C	30,000
			10 A, 250 VAC, (general use) at 40°C	
			TV-8 (NO only) at 40°C	25,000
			16 A, 250 VAC, (general use) (NO only) at 40°C	30,000
			12 A, 250 VAC, (general use) (NC only) at 40°C	

CSA Certified: (File No. LR31928)

Model	Contact form	Coil ratings	Contact ratings	Number of test operations
G5LE	SPDT-NO (1a) SPDT (1c)	5 to 24 VDC	10 A, 250 VAC (general use) at 40°C	6,000
			8 A, 30 VDC (resistive load) at 40°C	
			TV-3 (N.O only) at 40°C	25,000
G5LE-E			13 A, 120 VAC, (resistive load) (NO only) at 85°C	30,000
			10 A, 250 VAC, (general use) at 40°C	
			TV-8 (NO only) at 40°C	25,000
			16 A, 250 VAC, (general use) (NO only) at 40°C	30,000
			12 A, 250 VAC, (general use) (NC only) at 40°C	

VDE EN/IEC Certified: (Certificate No. 6850)

Model	Contact form	Coil ratings	Contact ratings	Number of test operations
G5LE	SPDT-NO (1a) SPDT (1c)	5, 12, 24 VDC	10 A, 250 VAC (cosϕ = 1) 85°C	50,000
G5LE-E			16 A, 250 VAC (cosϕ = 1) (NO only), 1s ON/5s OFF, 85°C	

TÜV EN/IEC Certified: (Certificate No. R50158258)

Model	Contact form	Coil ratings	Contact ratings	Number of test operations
G5LE	SPDT-NO (1a) SPDT (1c)	5, 12, 24 VDC	2.5 A, 250 VAC (cosϕ = 0.4) 85°C	100,000
			10 A, 250 VAC (resistive load) at 85°C	50,000
			8 A, 30 VAC (resistive load) at 40°C	100,000

■Precautions

- **Please refer to “PCB Relays Common Precautions” for correct use.**

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Cat. No. K100-E1-08
0318(0207)(O)

MCP23017/MCP23S17

16-Bit I/O Expander with Serial Interface

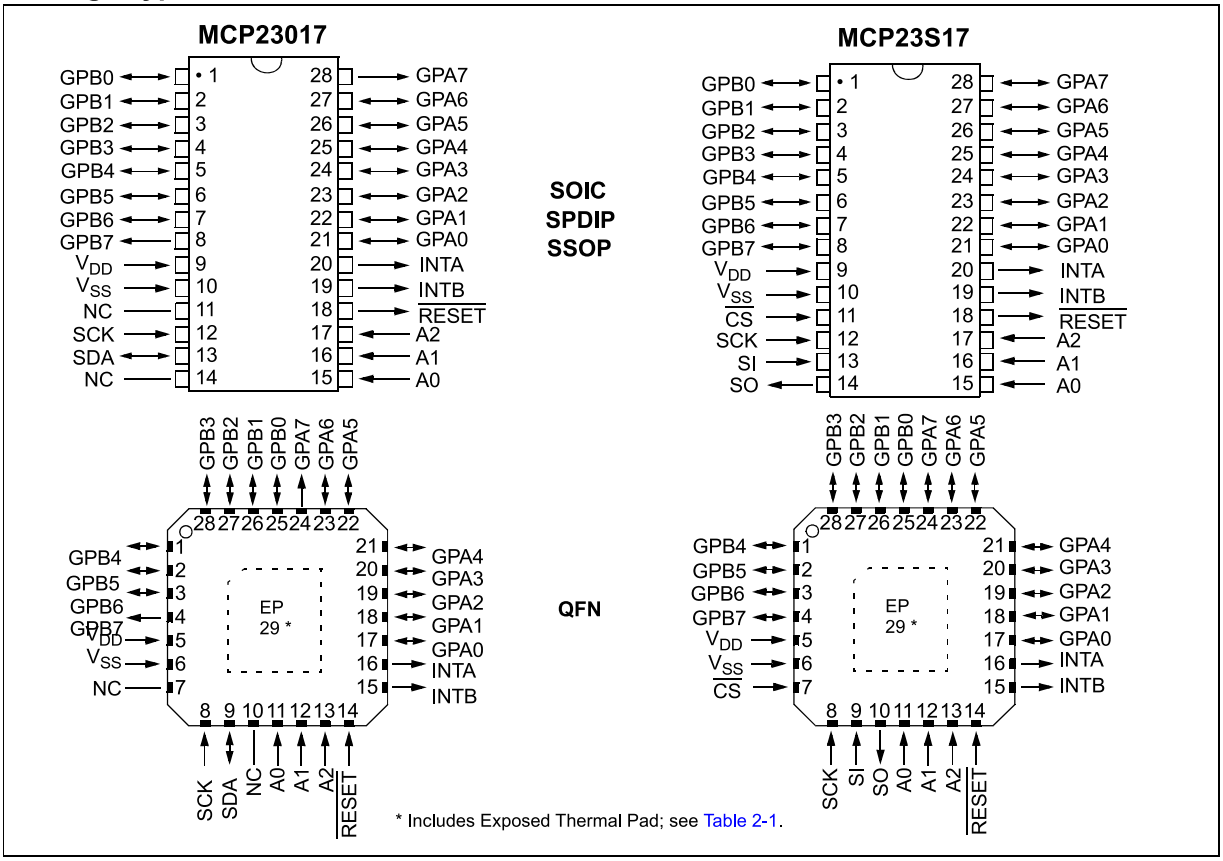
Features

- AEC-Q100 Qualified
- 16-Bit Remote Bidirectional I/O Port (Pins GPA7, GPB7 are output only for **MCP23017**):
  - I/O pins default to input
- High-Speed I^2C Interface (**MCP23017**):
  - 100 kHz
  - 400 kHz
  - 1.7 MHz
- High-Speed SPI Interface (**MCP23S17**):
  - 10 MHz (maximum)
- Three Hardware Address Pins to Allow Up to Eight Devices On the Bus
- Configurable Interrupt Output Pins:
  - Configurable as active-high, active-low or open-drain
- INTA and INTB Can Be Configured to Operate Independently or Together
- Configurable Interrupt Source:
  - Interrupt-on-change from configured register defaults or pin changes
- Polarity Inversion Register to Configure the Polarity of the Input Port Data
- External Reset Input
- Low Standby Current: 1 µA (max.)
- Operating Voltage:
  - 1.8V to 5.5V @ –40°C to +85°C
  - 2.7V to 5.5V @ –40°C to +125°C

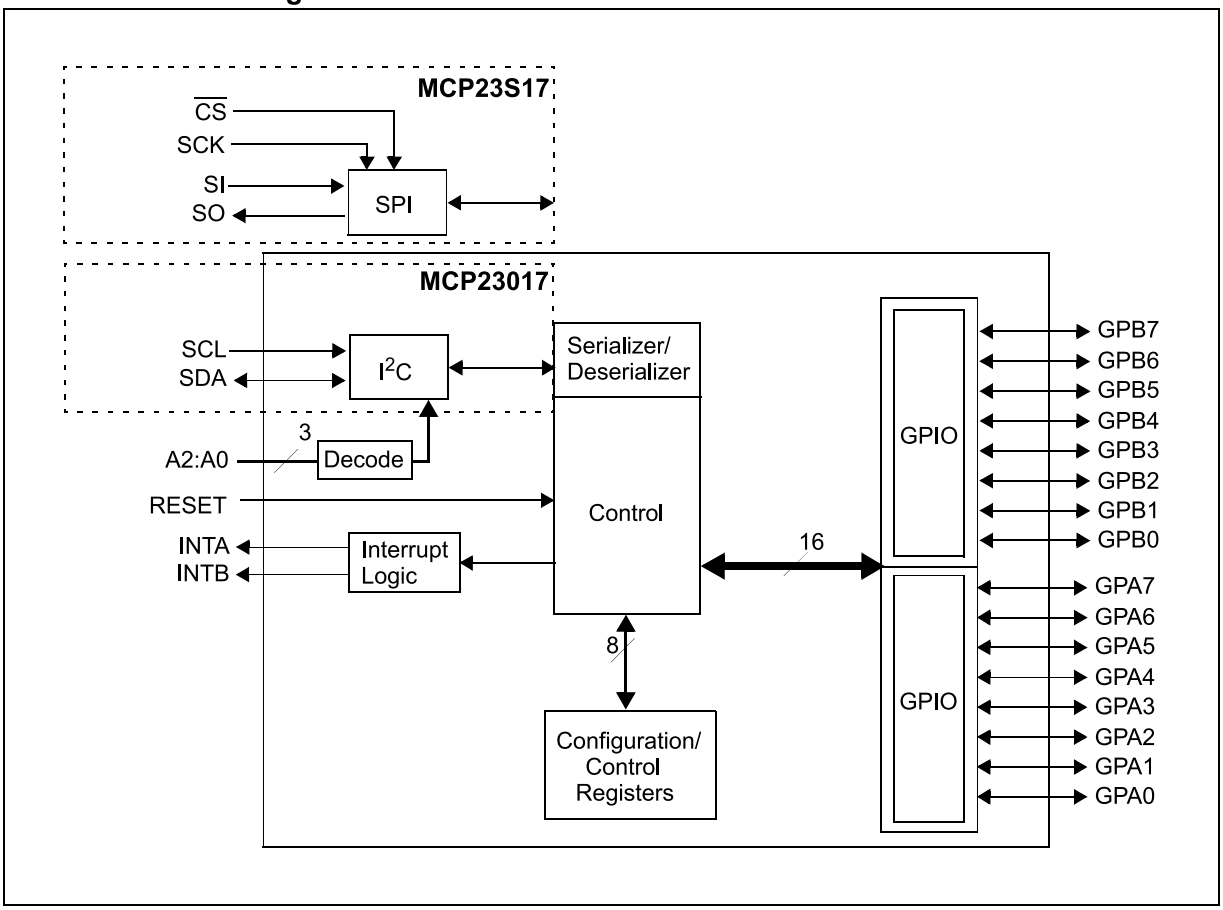
Packages

- 28-pin QFN, 6 x 6 mm Body
- 28-pin SOIC, Wide, 7.50 mm Body
- 28-pin SPDIP, 300 mil Body
- 28-pin SSOP, 5.30 mm Body

Package Types



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... –40°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... –0.3V to +5.5V
Voltage on all other pins with respect to V_{SS} (except V_{DD}) ..... –0.6V to (V_{DD} + 0.6V)
Total power dissipation ..... 700 mW
Maximum current out of V_{SS} pin ..... 150 mA
Maximum current into V_{DD} pin ..... 125 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any output pin ..... 25 mA
Maximum output current sourced by any output pin ..... 25 mA
ESD protection on all pins (HBM:MM) 4 kV:400V

† **Notice**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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1.1 DC Characteristics

TABLE 1-1: DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D001	Supply Voltage	V_{DD}	1.8	—	5.5	V	
D002	V_{DD} Start Voltage to ensure Power-on Reset	V_{POR}	—	V_{SS}	—	V	
D003	V_{DD} Rise Rate to ensure Power-on Reset	SV_{DD}	0.05	—	—	V/ms	Design guidance only. Not tested.
D004	Supply Current	I_{DD}	—	—	1	mA	SCL/SCK = 1 MHz
D005	Standby current	I_{DDS8}	—	—	1	µA	–40°C ≤ T_A ≤ +85°C
			—	—	3	µA	4.5V ≤ V_{DD} ≤ 5.5V +85°C ≤ T_A ≤+125°C (Note 1)
Input Low Voltage							
D030	A0, A1, A2 (TTL buffer)	V_{IL}	V_{SS}	—	0.15 V_{DD}	V	
D031	$\overline{CS}$, GPIO, SCL/SCK, SDA, $\overline{RESET}$ (Schmitt Trigger)	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
Input High Voltage							
D040	A0, A1, A2 (TTL buffer)	V_{IH}	0.25 V_{DD} + 0.8	—	V_{DD}	V	
D041	$\overline{CS}$, GPIO, SCL/SCK, SDA, $\overline{RESET}$ (Schmitt Trigger)	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	For entire V_{DD} range
Input Leakage Current							
D060	I/O port pins	I_{IL}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
Output Leakage Current							
D065	I/O port pins	I_{LO}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
D070	GPIO weak pull-up current	I_{PU}	40	75	115	µA	V_{DD} = 5V GP pins = V_{SS}
Output Low-Voltage							
D080	GPIO	V_{OL}	—	—	0.6	V	I_{OL} = 8.0 mA V_{DD} = 4.5V
	INT	V_{OL}	—	—	0.6	V	I_{OL} = 1.6 mA V_{DD} = 4.5V
	SO, SDA	V_{OL}	—	—	0.6	V	I_{OL} = 3.0 mA V_{DD} = 1.8V
	SDA	V_{OL}	—	—	0.8	V	I_{OL} = 3.0 mA V_{DD} = 4.5V
Output High-Voltage							
D090	GPIO, INT, SO	V_{OH}	V_{DD} – 0.7	—	—	V	I_{OH} = –3.0 mA V_{DD} = 4.5V
			V_{DD} – 0.7	—	—		I_{OH} = –400 µA V_{DD} = 1.8V
Capacitive Loading Specs on Output Pins							
D101	GPIO, SO, INT	C_{IO}	—	—	50	pF	
D102	SDA	C_B	—	—	400	pF	

Note 1: This parameter is characterized, not 100% tested.

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1.2 AC Characteristics

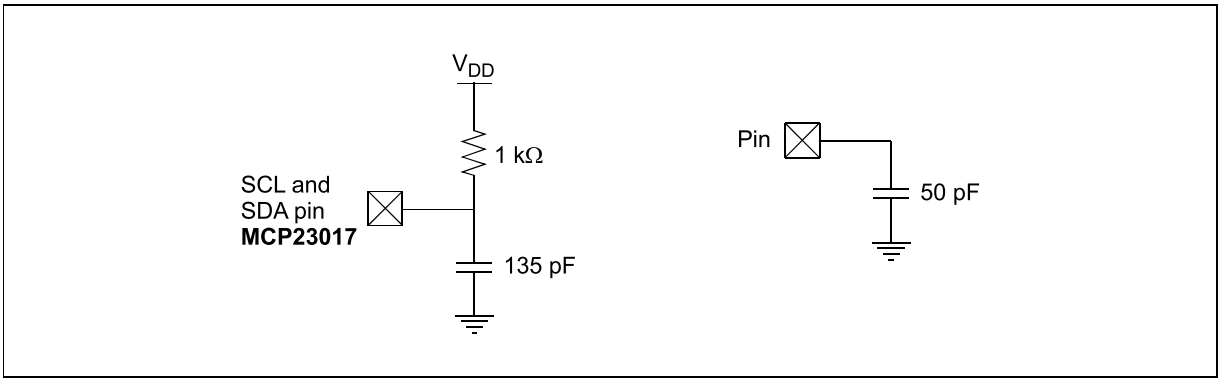


FIGURE 1-1: *Load Conditions for device Timing Specifications.*

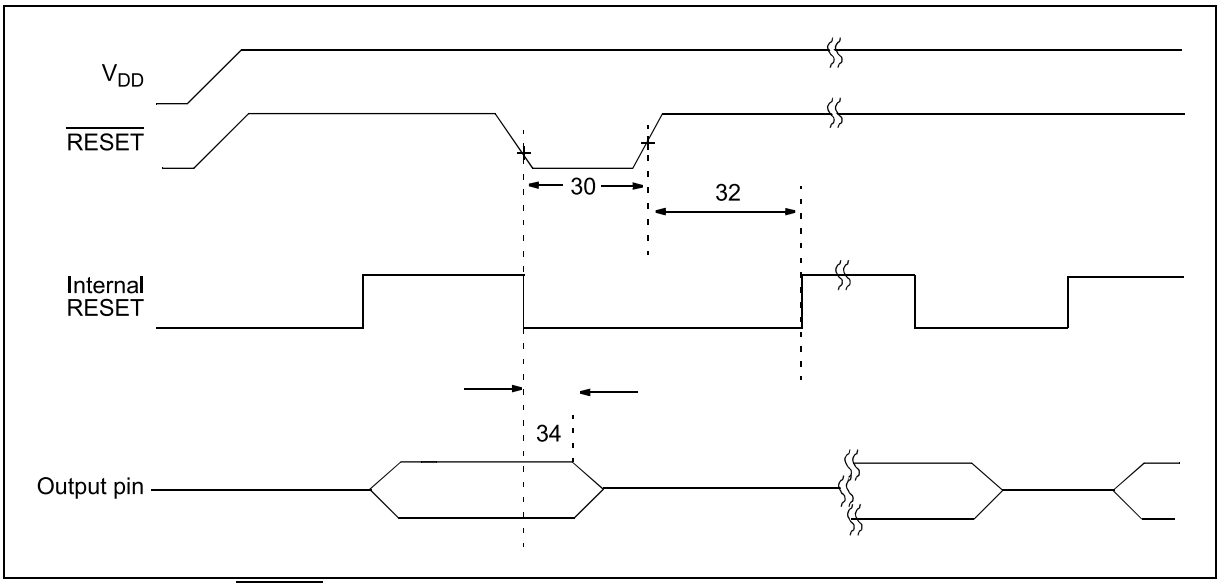


FIGURE 1-2: *$\overline{RESET}$ and Device Reset Timer Timing.*

TABLE 1-2: DEVICE RESET SPECIFICATIONS

AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ. (1)**	**Max.**	**Units**	**Conditions**
30	$\overline{RESET}$ Pulse Width (Low)	T_{RSTL}	1	—	—	µs	
32	Device Active After Reset high	T_{HLD}	—	0	—	ns	V_{DD} = 5.0V
34	Output High-Impedance From $\overline{RESET}$ Low	T_{IOZ}	—	—	1	µs	

Note 1: This parameter is characterized, not 100% tested.

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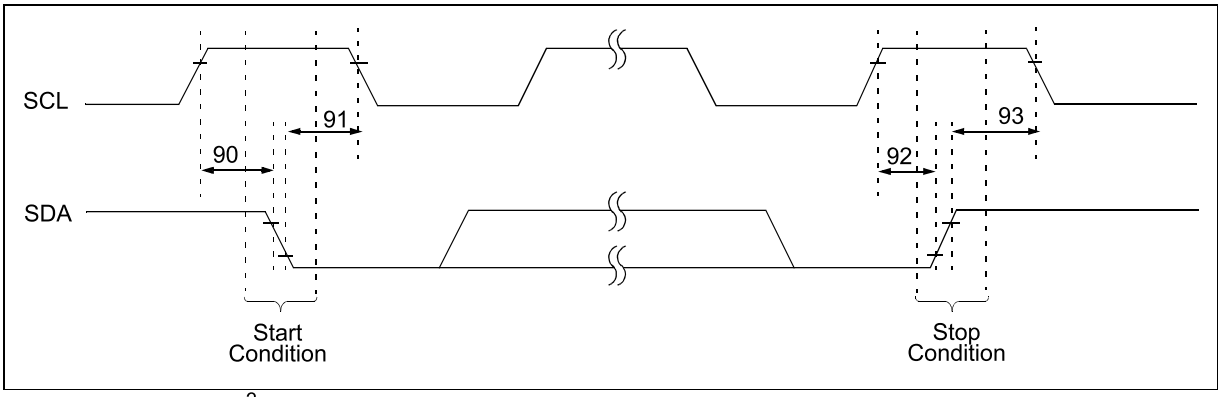


FIGURE 1-3: *I^2C Bus Start/Stop Bits Timing.*

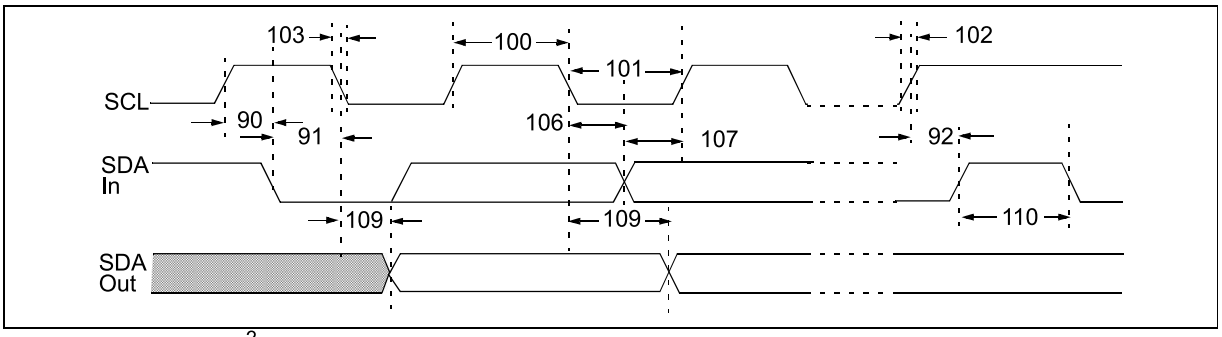


FIGURE 1-4: *I^2C Bus Data Timing.*

TABLE 1-3: I^2C BUS DATA REQUIREMENTS

I^2C Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C, R_{PU} (SCL, SDA) = 1 kΩ, C_L (SCL, SDA) = 135 pF							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
100	Clock High Time:	T_{HIGH}					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.12	—	—	µs	4.5V – 5.5V
101	Clock Low Time:	T_{LOW}					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.32	—	—	µs	4.5V – 5.5V
102	SDA and SCL Rise Time:	T_R (1)					
	100 kHz mode		—	—	1000	ns	1.8V – 5.5V
	400 kHz mode		20 + 0.1 C_B (2)	—	300	ns	2.7V – 5.5V
	1.7 MHz mode		20	—	160	ns	4.5V – 5.5V
103	SDA and SCL Fall Time:	T_F (1)					
	100 kHz mode		—	—	300	ns	1.8V – 5.5V
	400 kHz mode		20 + 0.1 C_B (2)	—	300	ns	2.7V – 5.5V
	1.7 MHz mode		20	—	80	ns	4.5V – 5.5V

Note 1: This parameter is characterized, not 100% tested.

2: C_B is specified to be from 10 to 400 pF.

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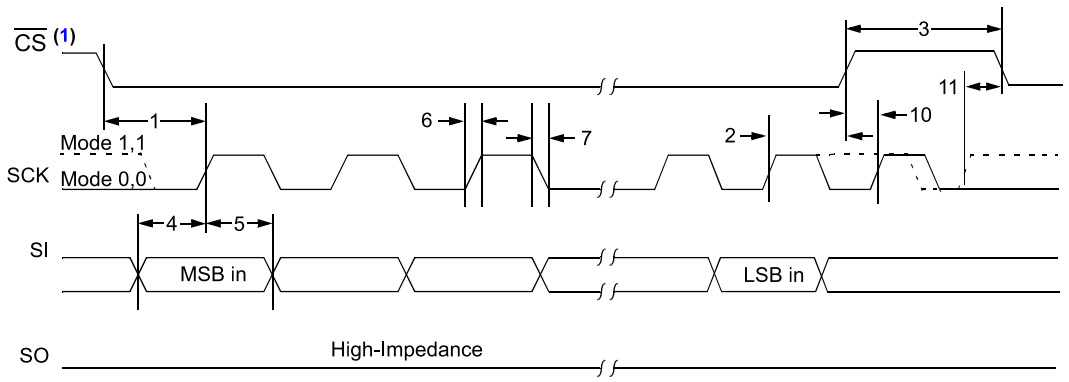
TABLE 1-3: I²C BUS DATA REQUIREMENTS (CONTINUED)

I²C Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C, R_{PU} (SCL, SDA) = 1 kΩ, C_L (SCL, SDA) = 135 pF							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
90	START Condition Setup Time:	$T_{SU:STA}$					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V
91	START Condition Hold Time:	$T_{HD:STA}$					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V
106	Data Input Hold Time:	$T_{HD:DAT}$					
	100 kHz mode		0	—	3.45	µs	1.8V – 5.5V
	400 kHz mode		0	—	0.9	µs	2.7V – 5.5V
	1.7 MHz mode		0	—	0.15	µs	4.5V – 5.5V
107	Data Input Setup Time:	$T_{SU:DAT}$					
	100 kHz mode		250	—	—	ns	1.8V – 5.5V
	400 kHz mode		100	—	—	ns	2.7V – 5.5V
	1.7 MHz mode		0.01	—	—	µs	4.5V – 5.5V
92	Stop Condition Setup Time:	$T_{SU:STO}$					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V–5.5V
109	Output Valid From Clock:	T_{AA}					
	100 kHz mode		—	—	3.45	µs	1.8V – 5.5V
	400 kHz mode		—	—	0.9	µs	2.7V – 5.5V
	1.7 MHz mode		—	—	0.18	µs	4.5V – 5.5V
110	Bus Free Time:	T_{BUF}					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		N/A	—	N/A	µs	4.5V – 5.5V
111	Bus Capacitive Loading:	C_B					
	100 kHz and 400 kHz		—	—	400	pF	**Note 1**
	1.7 MHz		—	—	100	pF	**Note 1**
112	Input Filter Spike Suppression (SDA and SCL):	T_{SP}					
	100 kHz and 400 kHz		—	—	50	ns	
	1.7 MHz		—	—	10	ns	Spike suppression off

Note 1: This parameter is characterized, not 100% tested.

2: C_B is specified to be from 10 to 400 pF.

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Note 1: When using SPI Mode 1,1 the $\overline{CS}$ pin needs to be toggled once before the first communication after power-up.

FIGURE 1-5: *SPI Input Timing.*

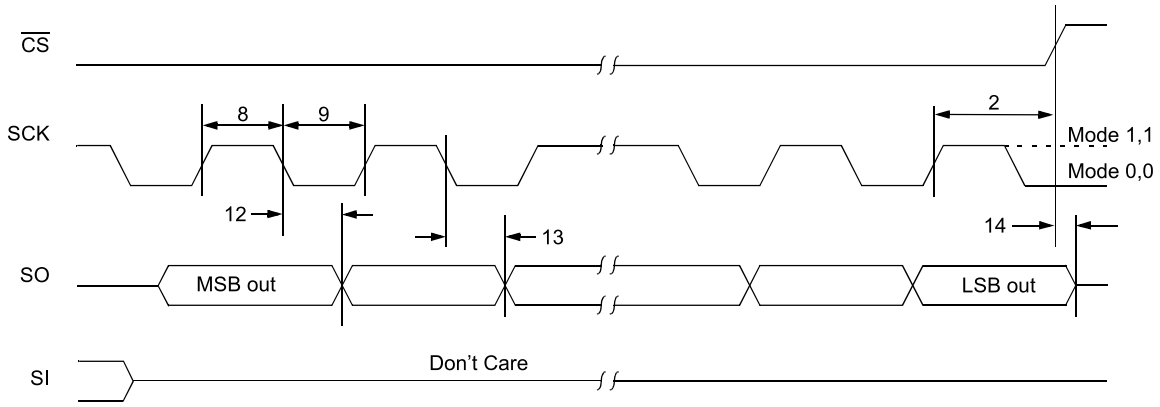


FIGURE 1-6: *SPI Output Timing.*

TABLE 1-4: SPI INTERFACE REQUIREMENTS

SPI Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
—	Clock Frequency	F_{CLK}	—	—	5	MHz	1.8V – 5.5V
			—	—	10	MHz	2.7V – 5.5V
			—	—	10	MHz	4.5V – 5.5V
1	$\overline{CS}$ Setup Time	T_{CSS}	50	—	—	ns	
2	$\overline{CS}$ Hold Time	T_{CSH}	100	—	—	ns	1.8V – 5.5V
			50	—	—	ns	2.7V – 5.5V
3	$\overline{CS}$ Disable Time	T_{CSD}	100	—	—	ns	1.8V – 5.5V
			50	—	—	ns	2.7V – 5.5V
4	Data Setup Time	T_{SU}	20	—	—	ns	1.8V – 5.5V
			10	—	—	ns	2.7V – 5.5V

Note 1: This parameter is characterized, not 100% tested.

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TABLE 1-4: SPI INTERFACE REQUIREMENTS (CONTINUED)

SPI Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
5	Data Hold Time	T_{HD}	20	—	—	ns	1.8V – 5.5V
			10	—	—	ns	2.7V – 5.5V
6	CLK Rise Time	T_R	—	—	2	µs	**Note 1**
7	CLK Fall Time	T_F	—	—	2	µs	**Note 1**
8	Clock High Time	T_{HI}	90	—	—	ns	1.8V – 5.5V
			45	—	—	ns	2.7V – 5.5V
9	Clock Low Time	T_{LO}	90	—	—	ns	1.8V – 5.5V
			45	—	—	ns	2.7V – 5.5V
10	Clock Delay Time	T_{CLD}	50	—	—	ns	
11	Clock Enable Time	T_{CLE}	50	—	—	ns	
12	Output Valid from Clock Low	T_V	—	—	90	ns	1.8V – 5.5V
			—	—	45	ns	2.7V – 5.5V
13	Output Hold Time	T_{HO}	0	—	—	ns	
14	Output Disable Time	T_{DIS}	—	—	100	ns	

Note 1: This parameter is characterized, not 100% tested.

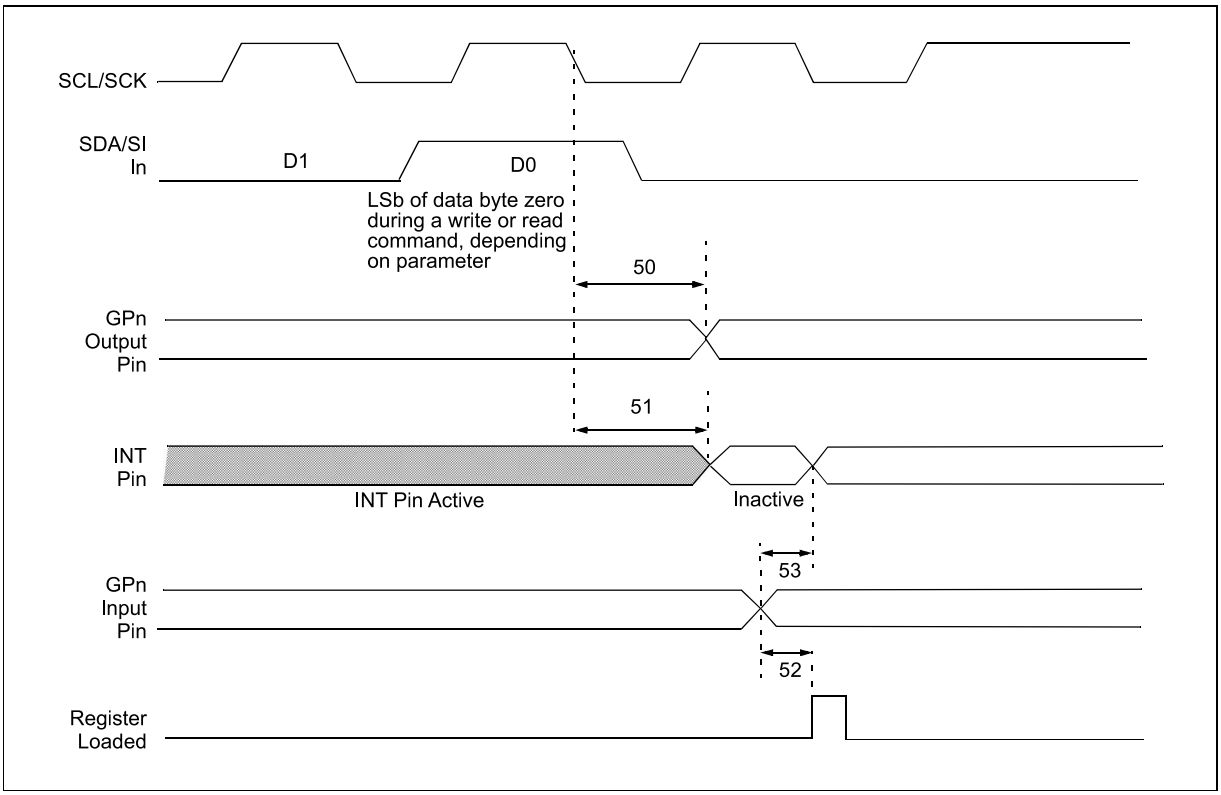


FIGURE 1-7: *GPIO and INT Timing.*

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TABLE 1-5: GP AND INT PINS REQUIREMENTS

GP and INT Pins AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at –40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
50	Serial Data to Output Valid	T_{GPOV}	—	—	500	ns	
51	Interrupt Pin Disable Time	T_{INTD}	—	—	600	ns	
52	GP Input Change to Register Valid	T_{GPIV}	—	—	450	ns	
53	IOC Event to INT Active	T_{GPINT}	—	—	600	ns	
	Glitch Filter on GP Pins	T_{GLITCH}	—	—	150	ns	**Note 1**

Note 1: This parameter is characterized, not 100% tested.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PINOUT DESCRIPTION

Pin Name	QFN	SOIC SPDIP SSOP	Pin Type	Function
GPB0	25	1	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB1	26	2	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB2	27	3	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB3	28	4	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB4	1	5	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB5	2	6	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB6	3	7	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB7	4	8	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor./ Output only (**MCP23017**).
V_{DD}	5	9	P	Power
V_{SS}	6	10	P	Ground
NC/$\overline{CS}$	7	11	I	NC (**MCP23017**)/Chip Select (**MCP23S17**)
SCK	8	12	I	Serial clock input
SDA/SI	9	13	I/O	Serial data I/O (**MCP23017**)/Serial data input (**MCP23S17**)
NC/SO	10	14	O	NC (**MCP23017**)/Serial data out (**MCP23S17**)
A0	11	15	I	Hardware address pin. Must be externally biased.
A1	12	16	I	Hardware address pin. Must be externally biased.
A2	13	17	I	Hardware address pin. Must be externally biased.
$\overline{RESET}$	14	18	I	Hardware reset. Must be externally biased.
INTB	15	19	O	Interrupt output for PORTB. Can be configured as active-high, active-low or open-drain.
INTA	16	20	O	Interrupt output for PORTA. Can be configured as active-high, active-low or open-drain.
GPA0	17	21	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA1	18	22	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA2	19	23	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA3	20	24	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA4	21	25	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA5	22	26	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA6	23	27	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA7	24	28	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor./ Output only (**MCP23017**).
EP	29	—	—	Exposed Thermal Pad. Either connect to V_{SS}, or leave unconnected.

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3.0 DEVICE OVERVIEW

MCP23017/MCP23S17 (MCP23X17) device family provides 16-bit, general purpose parallel I/O expansion for I^2C bus or SPI applications. The two devices differ only in the serial interface:

- MCP23017 – I^2C interface
- MCP23S17 – SPI interface

MCP23X17 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system host can enable the I/Os as either inputs or outputs by writing the I/O configuration bits (IODIRA/B). The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system host.

The 16-bit I/O port functionally consists of two 8-bit ports (PORTA and PORTB). MCP23X17 can be configured to operate in the 8-bit or 16-bit modes via IOCON.BANK.

There are two interrupt pins, INTA and INTB, that can be associated with their respective ports, or can be logically OR'ed together so that both pins will activate if either port causes an interrupt.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding Input Port register state. This is used to indicate to the system host that an input state has changed.
2. When an input state differs from a preconfigured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

3.1 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until V_{DD} has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum V_{DD} rise time is specified in **Section 1.0 "Electrical Characteristics"**.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

3.2 Serial Interface

This block handles the functionality of the I^2C (**MCP23017**) or SPI (**MCP23S17**) interface protocol. MCP23X17 contains 22 individual registers (11 register pairs) that can be addressed through the Serial Interface block, as shown in Table 3-1.

TABLE 3-1: REGISTER ADDRESSES

Address IOCON.BANK = 1	Address IOCON.BANK = 0	Access to:
00h	00h	IODIRA
10h	01h	IODIRB
01h	02h	IPOLA
11h	03h	IPOLB
02h	04h	GPINTENA
12h	05h	GPINTENB
03h	06h	DEFVALA
13h	07h	DEFVALB
04h	08h	INTCONA
14h	09h	INTCONB
05h	0Ah	IOCON
15h	0Bh	IOCON
06h	0Ch	GPPUA
16h	0Dh	GPPUB
07h	0Eh	INTFA
17h	0Fh	INTFB
08h	10h	INTCAPA
18h	11h	INTCAPB
09h	12h	GPIOA
19h	13h	GPIOB
0Ah	14h	OLATA
1Ah	15h	OLATB

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3.2.1 BYTE MODE AND SEQUENTIAL MODE

MCP23X17 family has the ability to operate in Byte mode or Sequential mode (IOCON.SEQOP).

Byte mode disables automatic Address Pointer incrementing. When operating in Byte mode, MCP23X17 family does not increment its internal address counter after each byte during the data transfer. This gives the ability to continually access the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes or for continually writing to the output latches.

A special mode **(Byte mode with IOCON.BANK = 0)** causes the address pointer to toggle between associated A/B register pairs. For example, if the BANK bit is cleared and the Address Pointer is initially set to address 12h (GPIOA) or 13h (GPIOB), the pointer will toggle between GPIOA and GPIOB. Note that the Address Pointer can initially point to either address in the register pair.

Sequential mode enables automatic address pointer incrementing. When operating in Sequential mode, MCP23X17 family increments its address counter after each byte during the data transfer. The Address Pointer automatically rolls over to address 00h after accessing the last register.

These two modes are not to be confused with single writes/reads and continuous writes/reads that are serial protocol sequences. For example, the device may be configured for Byte mode and the host may perform a continuous read. In this case, MCP23X17 would not increment the Address Pointer and would repeatedly drive data from the same location.

3.2.2 I^2C INTERFACE

3.2.2.1 I^2C Write Operation

The I^2C write operation includes the control byte and register address sequence, as shown in Figure 3-1. This sequence is followed by eight bits of data from the host and an Acknowledge (ACK) from the MCP23017. The operation is ended with a Stop (P) or Restart (SR) condition being generated by the host.

Data is written to MCP23017 after every byte transfer. If a Stop or Restart condition is generated during a data transfer, the data will not be written to MCP23017.

Both “byte writes” and “sequential writes” are supported by MCP23017. If Sequential mode is enabled (IOCON, SEQOP = 0) (default), MCP23017 increments its address counter after each ACK during the data transfer.

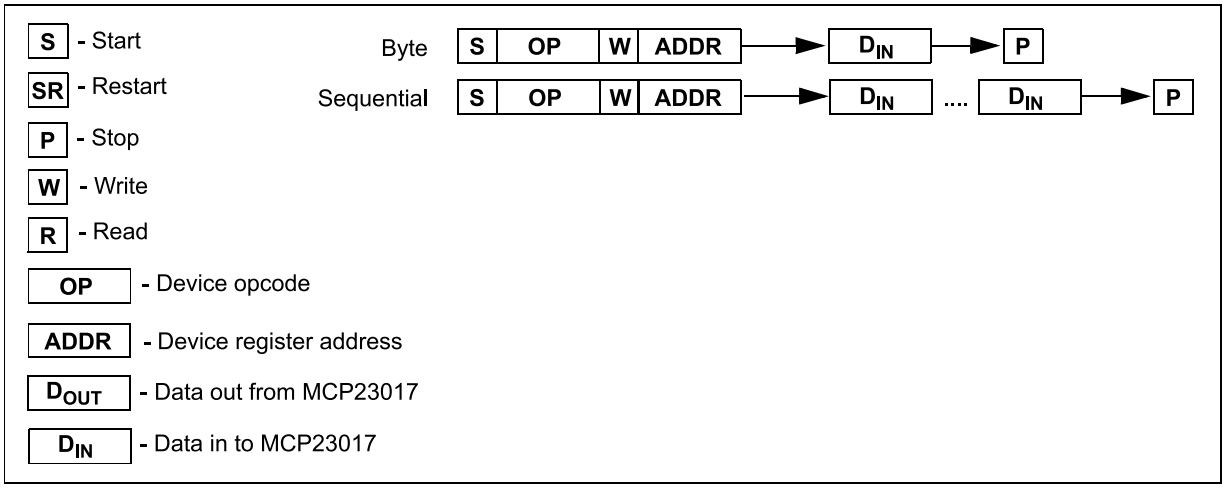


FIGURE 3-1: *Byte and Sequential Write.*

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3.2.2.2 I²C Read Operation

I²C Read operations include the control byte sequence, as shown in Figure 3-2. This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit set (R/W = 1). The MCP23017 then transmits the data contained in the addressed register. The sequence is ended with the host generating a Stop or Restart condition.

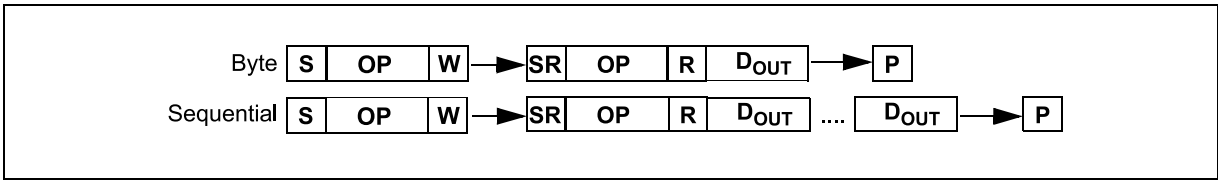


FIGURE 3-2: *Byte and Sequential Read.*

3.2.2.3 I²C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the host clocks the next byte pointed to by the address pointer (see **Section 3.2.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends with the host sending a Stop or Restart condition.

MCP23017 Address Pointer will roll over to address zero after reaching the last register address. Refer to Figure 3-3.

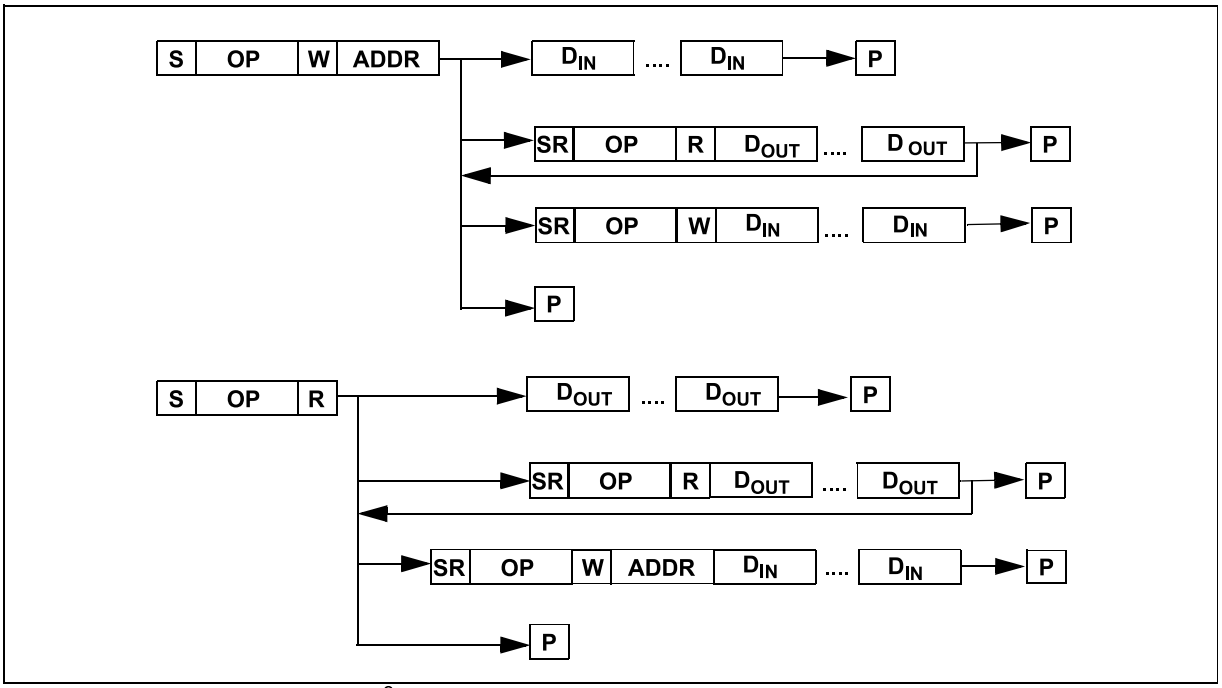


FIGURE 3-3: *MCP23017 I²C Device Protocol.*

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3.2.3 SPI INTERFACE

3.2.3.1 SPI Write Operation

The SPI write operation is started by lowering $\overline{CS}$. The Write command (client address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

3.2.3.2 SPI Read Operation

The SPI read operation is started by lowering $\overline{CS}$. The SPI read command (client address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

3.2.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising $\overline{CS}$, the host clocks the next byte pointed to by the Address Pointer. (see **Section 3.2.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends by the raising of $\overline{CS}$.

MCP23S17 Address Pointer will roll over to address zero after reaching the last register address.

3.3 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state. The pins must be biased externally.

3.3.1 ADDRESSING I²C DEVICES (**MCP23017**)

MCP23017 is a client I²C interface device that supports 7-bit client addressing, with the read/write bit filling out the control byte. The client address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 3-4 shows the control byte format.

3.3.2 ADDRESSING SPI DEVICES (**MCP23S17**)

MCP23S17 is a client SPI device. The client address contains four fixed bits and three user-defined hardware address bits (if enabled via IOCON.HAEN) (pins A2, A1 and A0) with the read/write bit filling out the control byte. Figure 3-5 shows the control byte format. The address pins should be externally biased even if disabled (IOCON.HAEN = 0).

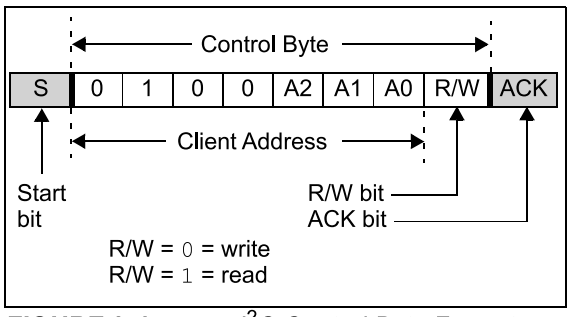


FIGURE 3-4: *I²C Control Byte Format.*

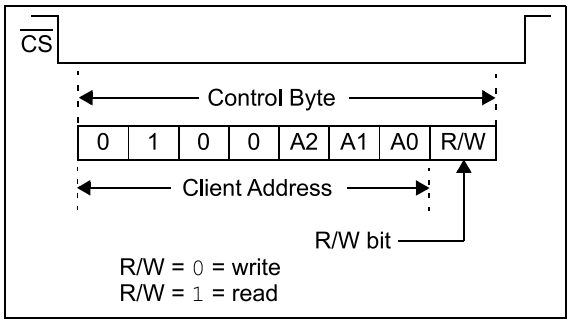


FIGURE 3-5: *SPI Control Byte Format.*

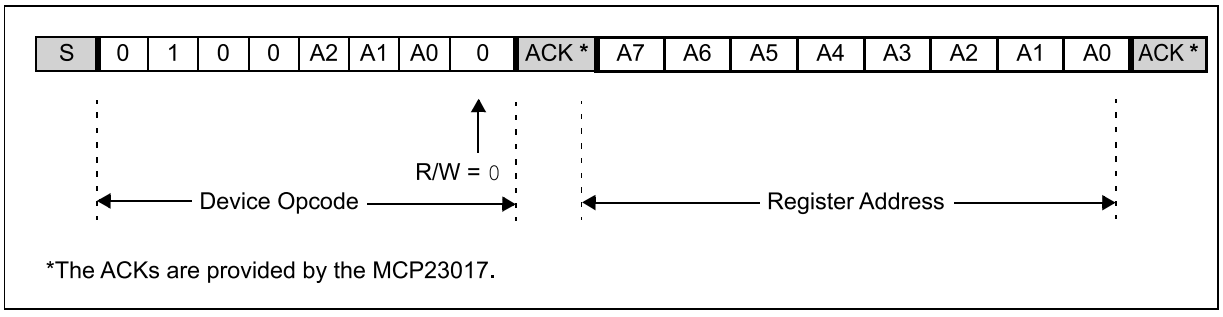


FIGURE 3-6: *I²C Addressing Registers.*

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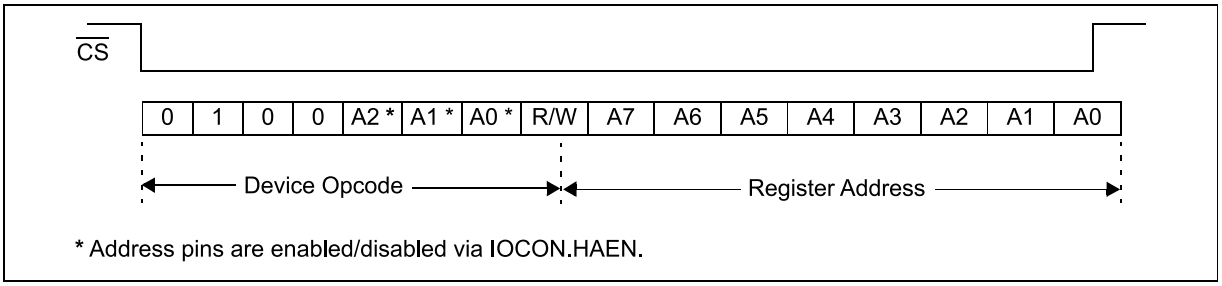


FIGURE 3-7: *SPI Addressing Registers.*

3.4 GPIO Port

The GPIO module is a general purpose, 16-bit wide, bidirectional port that is functionally split into two 8-bit wide ports.

The GPIO module contains the data ports (GPIOn), internal pull-up resistors and the output latches (OLATn).

Reading the GPIOn register reads the value on the port. Reading the OLATn register only reads the latches, not the actual value on the port.

Writing to the GPIOn register actually causes a write to the latches (OLATn). Writing to the OLATn register forces the associated output drivers to drive to the level in OLATn. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 1)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUA	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOA	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
IODIRB	10	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLB	11	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENB	12	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUB	16	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOB	19	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATB	1A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

TABLE 3-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 0)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IODIRB	01	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	02	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
IPOLB	03	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	04	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPINTENB	05	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUA	0C	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPPUB	0D	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOA	12	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
GPIOB	13	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	14	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
OLATB	15	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

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3.5 Configuration and Control Registers

There are 21 registers associated with the MCP23X17, as shown in Tables 3-4 and 3-5. The two tables show the register mapping with the two BANK bit values. Ten registers are associated with PORTA and ten are associated with PORTB. One register (IOCON) is shared between the two ports. The PORTA registers are identical to the PORTB registers, therefore, they will be referred to without differentiating between the port designation (i.e., they will not have the “A” or “B” designator assigned) in the register tables.

TABLE 3-4: CONTROL REGISTER SUMMARY (IOCON.BANK = 1)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALA	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONA	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUA	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTFA	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPA	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOA	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
IODIRB	10	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLB	11	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENB	12	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALB	13	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONB	14	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	15	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUB	16	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTFB	17	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPB	18	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOB	19	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATB	1A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

TABLE 3-5: CONTROL REGISTER SUMMARY (IOCON.BANK = 0)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IODIRB	01	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	02	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
IPOLB	03	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	04	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPINTENB	05	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALA	06	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
DEFVALB	07	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONA	08	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
INTCONB	09	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	0A	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
IOCON	0B	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUA	0C	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPPUB	0D	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000

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TABLE 3-5: CONTROL REGISTER SUMMARY (IOCON.BANK = 0) (CONTINUED)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
INTFA	0E	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTFB	0F	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPA	10	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
INTCAPB	11	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOA	12	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
GPIOB	13	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	14	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
OLATB	15	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

3.5.1 I/O DIRECTION REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

IODIR: I/O DIRECTION REGISTER (ADDR 0x00)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IO<7:0>:** Controls the direction of data I/O <7:0>
1 = Pin is configured as an input.
0 = Pin is configured as an output.

Note: For **MCP23017**, IO7 must be set via I^2C interface to "0" (output).

3.5.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 3-1: IPOL: INPUT POLARITY PORT REGISTER (ADDR 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IP<7:0>:** Controls the polarity inversion of the input pins <7:0>
1 = GPIO register bit reflects the opposite logic state of the input pin.
0 = GPIO register bit reflects the same logic state of the input pin.

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3.5.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 3-2: GPINTEN: INTERRUPT-ON-CHANGE PINS (ADDR 0x02) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **GPINT<7:0>:** General purpose I/O interrupt-on-change bits <7:0>
1 = Enables GPIO input pin for interrupt-on-change event.
0 = Disables GPIO input pin for interrupt-on-change event.

Note 1: Refer to INTCON.

3.5.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 3-3: DEFVAL: DEFAULT VALUE REGISTER (ADDR 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DEF<7:0>:** Sets the compare value for pins configured for interrupt-on-change from defaults <7:0> **(Note 1)**
If the associated pin level is the opposite from the register bit, an interrupt occurs. **(Note 2)**

Note 1: Refer to INTCON.
2: Refer to INTCON and GPINTEN.

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3.5.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 3-4: INTCON: INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IOC<7:0>:** Controls how the associated pin value is compared for interrupt-on-change <7:0>
1 = Pin value is compared against the associated bit in the DEFVAL register.
0 = Pin value is compared against the previous pin value.

Note 1: Refer to INTCON and GPINTEN.

3.5.6 CONFIGURATION REGISTER

The IOCON register contains several bits for configuring the device:

The BANK bit changes how the registers are mapped (see Tables 3-4 and 3-5 for more details).

- If BANK = 1, the registers associated with each port are segregated. Registers associated with PORTA are mapped from address 00h - 0Ah and registers associated with PORTB are mapped from 10h - 1Ah.
- If BANK = 0, the A/B registers are paired. For example, IODIRA is mapped to address 00h and IODIRB is mapped to the next address (address 01h). The mapping for all registers is from 00h -15h.

It is important to take care when changing the BANK bit as the address mapping changes after the byte is clocked into the device. The address pointer may point to an invalid location after the bit is modified.

For example, if the device is configured to automatically increment its internal Address Pointer, the following scenario would occur:

- BANK = 0
- Write 80h to address 0Ah (IOCON) to set the BANK bit
- Once the write completes, the internal address now points to 0Bh which is an invalid address when the BANK bit is set.

For this reason, when changing the BANK bit, it is advised to only perform byte writes to this register.

The **MIRROR** bit controls how the INTA and INTB pins function with respect to each other.

- When MIRROR = 1, the INTn pins are functionally OR'ed so that an interrupt on either port will cause both pins to activate.
- When MIRROR = 0, the INT pins are separated. Interrupt conditions on a port will cause its respective INT pin to activate.

The Sequential Operation (**SEQOP**) controls the incrementing function of the Address Pointer. If the address pointer is disabled, the Address Pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.

The Slew Rate (**DISSLW**) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to low.

The Hardware Address Enable (**HAEN**) bit enables/disables hardware addressing on the MCP23S17 only. The address pins (A2, A1 and A0) must be externally biased, regardless of the HAEN bit value.

If enabled (HAEN = 1), the device's hardware address matches the address pins.

If disabled (HAEN = 0), the device's hardware address is A2 = A1 = A0 = 0.

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The Open-Drain (**ODR**) control bit enables/disables the INT pin for open-drain configuration. Setting this bit overrides the INTPOL bit.

The Interrupt Polarity (**INTPOL**) sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

REGISTER 3-5: IOCON: I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **BANK:** Controls how the registers are addressed
1 = The registers associated with each port are separated into different banks.
0 = The registers are in the same bank (addresses are sequential).

bit 6 **MIRROR:** INT Pins Mirror bit
1 = The INT pins are internally connected
0 = The INT pins are not connected. INTA is associated with PORTA and INTB is associated with PORTB

bit 5 **SEQOP:** Sequential Operation mode bit
1 = Sequential operation disabled, address pointer does not increment.
0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew Rate control bit for SDA output
1 = Slew rate disabled
0 = Slew rate enabled

bit 3 **HAEN:** Hardware Address Enable bit (**MCP23S17** only) **(Note 1)**
1 = Enables the MCP23S17 address pins.
0 = Disables the MCP23S17 address pins.

bit 2 **ODR:** Configures the INT pin as an open-drain output
1 = Open-drain output (overrides the INTPOL bit.)
0 = Active driver output (INTPOL bit sets the polarity.)

bit 1 **INTPOL:** This bit sets the polarity of the INT output pin
1 = Active-high
0 = Active-low

bit 0 **Unimplemented:** Read as '0'

Note 1: Address pins are always enabled on the MCP23017.

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3.5.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 kΩ resistor.

REGISTER 3-6: GPPU: GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PU<7:0>** Controls the weak pull-up resistors on each pin (when configured as an input)
1 = Pull-up enabled
0 = Pull-up disabled

3.5.8 INTERRUPT FLAG REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A set bit indicates that the associated pin caused the interrupt.

This register is read-only. Writes to this register will be ignored.

REGISTER 3-7: INTF: INTERRUPT FLAG REGISTER (ADDR 0x07)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **INT<7:0>:** Reflects the interrupt condition on the port. It reflects the change only if interrupts are enabled per GPINTEN<7:0>.
1 = Pin caused interrupt.
0 = Interrupt not pending

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3.5.9 INTERRUPT CAPTURED REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is read-only and is updated only when an interrupt occurs. The register remains unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 3-8: INTCAP: INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ICP<7:0>:** Reflects the logic level on the port pins at the time of interrupt due to pin change <7:0>
1 = Logic-high
0 = Logic-low

3.5.10 PORT REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 3-9: GPIO: GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **GP<7:0>:** Reflects the logic level on the pins <7:0>
1 = Logic-high
0 = Logic-low

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3.5.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modifies the pins configured as outputs.

REGISTER 3-10: OLAT: OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **OL<7:0>:** Reflects the logic level on the output latch <7:0>
1 = Logic-high
0 = Logic-low

3.6 Interrupt Logic

If enabled, MCP23X17 activates the INTn interrupt output when one of the port pins changes state or when a pin does not match the preconfigured default. Each pin is individually configurable as follows:

- Enable/disable interrupt via GPINTEN.
- Can interrupt on either pin change or change from default as configured in DEFVAL.

Both conditions are referred to as Interrupt-on-Change (IOC).

The interrupt control module uses the following registers/bits:

- IOCON.MIRROR – controls if the two interrupt pins mirror each other.
- GPINTEN – Interrupt enable register.
- INTCON – controls the source for the IOC.
- DEFVAL – contains the register default for IOC operation.

3.6.1 INTA AND INTB

There are two interrupt pins: INTA and INTB. By default, INTA is associated with GPAn pins (PORTA) and INTB is associated with GPBn pins (PORTB). Each port has an independent signal which is cleared if its associated GPIO or INTCAP register is read.

3.6.1.1 Mirroring the INT pins

Additionally, the INTn pins can be configured to mirror each other so that any interrupt will cause both pins to go active. This is controlled via IOCON.MIRROR.

If IOCON.MIRROR = 0, the internal signals are routed independently to the INTA and INTB pads.

If IOCON.MIRROR = 1, the internal signals are OR'ed together and routed to the INTn pads. In this case, the interrupt will only be cleared if the associated GPIO or INTCAP is read (see Table 3-6).

TABLE 3-6: INTERRUPT OPERATION (IOCON.MIRROR = 1)

Interrupt Condition	Read PORTn (1)	Interrupt Result
GPIOA	PORTA	Clear
	PORTB	Unchanged
GPIOB	PORTA	Unchanged
	PORTB	Clear
GPIOA and GPIOB	PORTA	Unchanged
	PORTB	Unchanged
	Both PORTA and PORTB	Clear

Note 1: PORTn = GPIOn or INTCAPn

3.6.2 IOC FROM PIN CHANGE

If enabled, MCP23X17 generates an interrupt if a mismatch condition exists between the current port value and the previous port value. Only IOC-enabled pins will be compared. Refer to Registers 3-2 and 3-4.

3.6.3 IOC FROM REGISTER DEFAULT

If enabled, MCP23X17 generates an interrupt if a mismatch occurs between the DEFVAL register and the port. Only IOC enabled pins are compared. Refer to Registers 3-2, 3-3 and 3-4.

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3.6.4 INTERRUPT OPERATION

The INTn interrupt output can be configured as active-low, active-high or open-drain via the IOCON register.

Only those pins that are configured as an input (IODIR register) with Interrupt-On-Change (IOC) enabled (IOINTEN register) can cause an interrupt. Pins defined as an output have no effect on the interrupt output pin.

Input change activity on a port input pin that is enabled for IOC generates an internal device interrupt and the device captures the value of the port and copies it into INTCAP. The interrupt remains active until the INTCAP or GPIO register is read. Writing to these registers does not affect the interrupt. The interrupt condition is cleared after the LSb of the data is clocked out during a read command of GPIO or INTCAP.

The first interrupt event causes the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

Note:	The value in INTCAP can be lost if GPIO is read before INTCAP while another IOC is pending. After reading GPIO, the interrupt will clear and then set due to the pending IOC, causing the INTCAP register to update.

3.6.5 INTERRUPT CONDITIONS

There are two possible configurations that cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs and after clearing the interrupt condition (i.e., after reading GPIO or INTCAP). For example, an interrupt occurs by an input changing from '1' to '0'. The new initial state for the pin is a logic '0' after the interrupt is cleared.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTCAP or GPIO is read.

See Figures 3-8 and 3-9 for more information on interrupt operations.

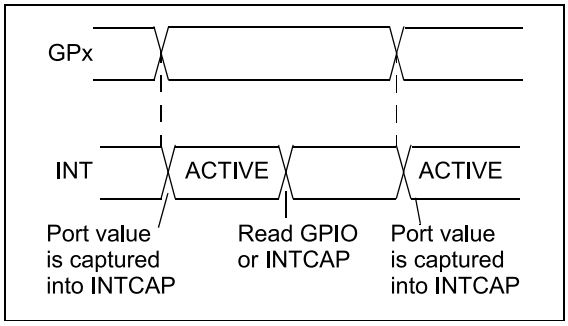


FIGURE 3-8: *Interrupt-on-Pin Change.*

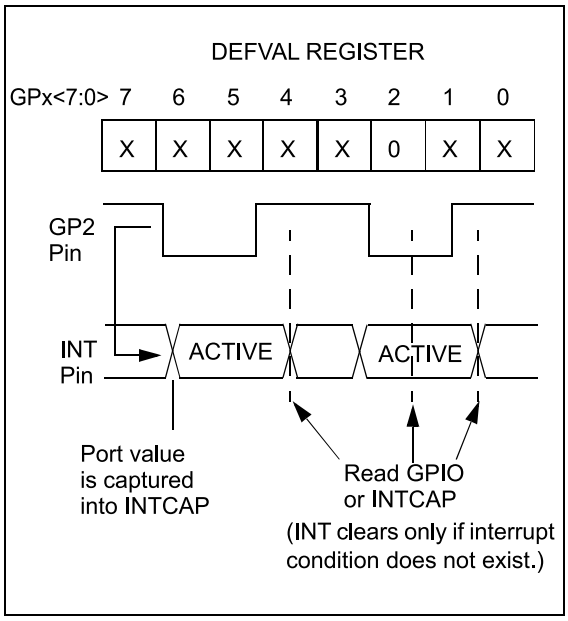


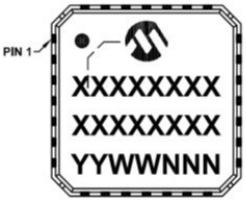
FIGURE 3-9: *Interrupt-on-Change from Register Default.*

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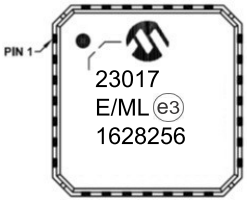
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

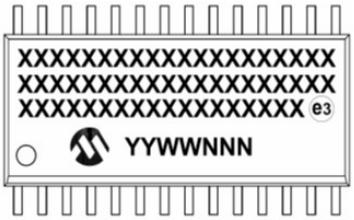
28-Lead QFN



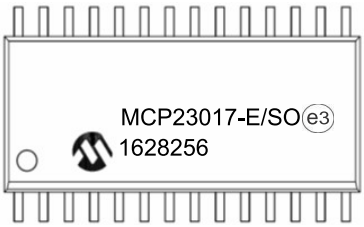
Example:



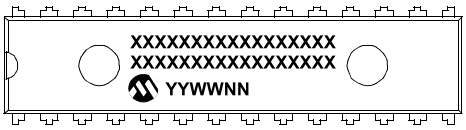
28-Lead SOIC



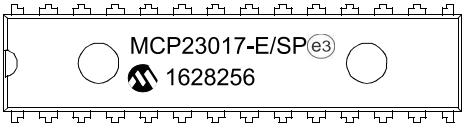
Example:



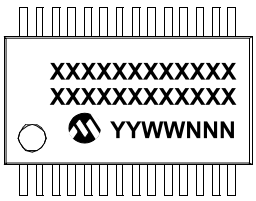
28-Lead SPDIP



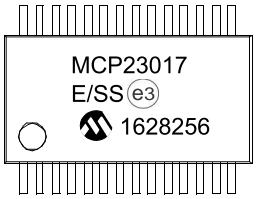
Example:



28-Lead SSOP



Example:



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

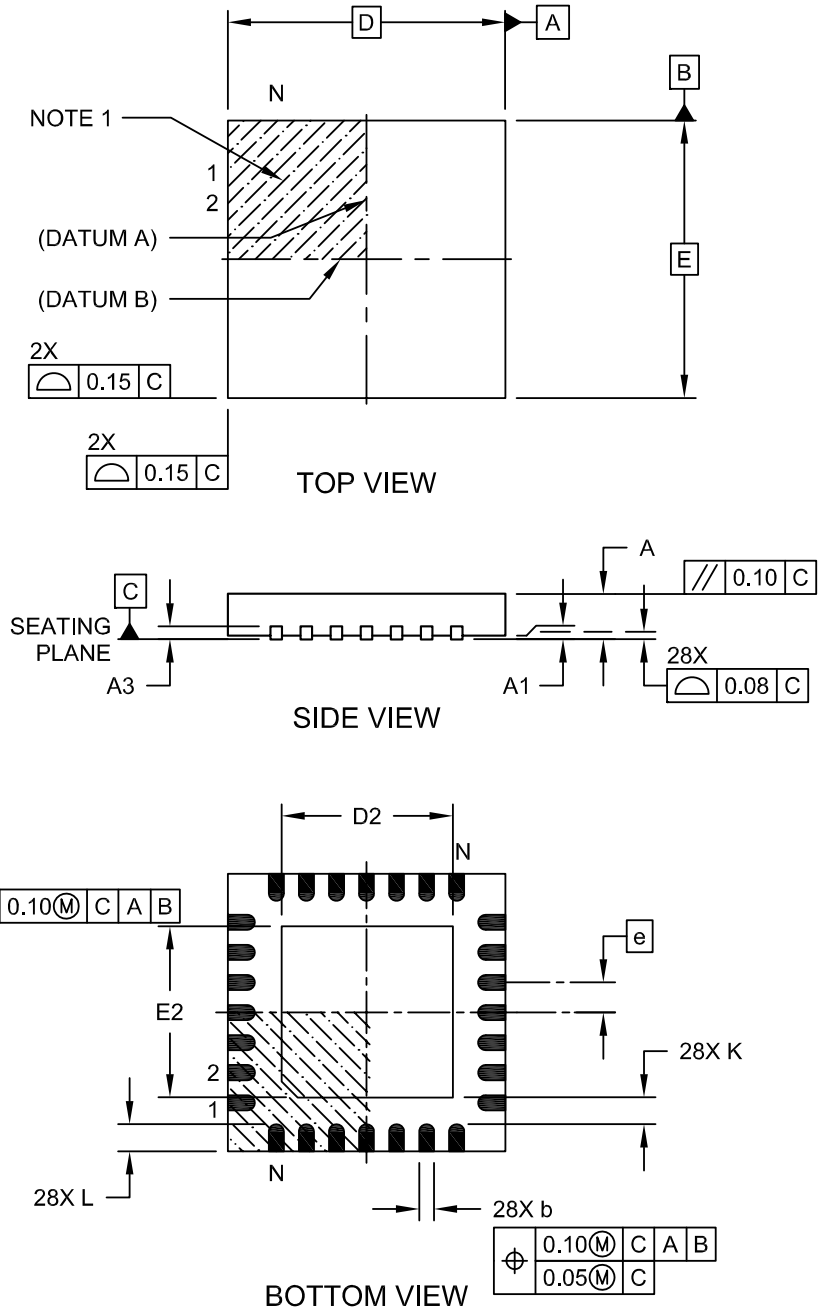
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

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28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

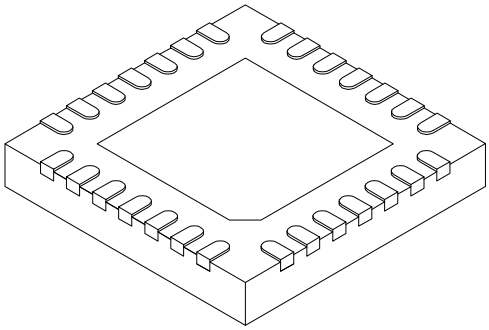


Microchip Technology Drawing C04-105C Sheet 1 of 2

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28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

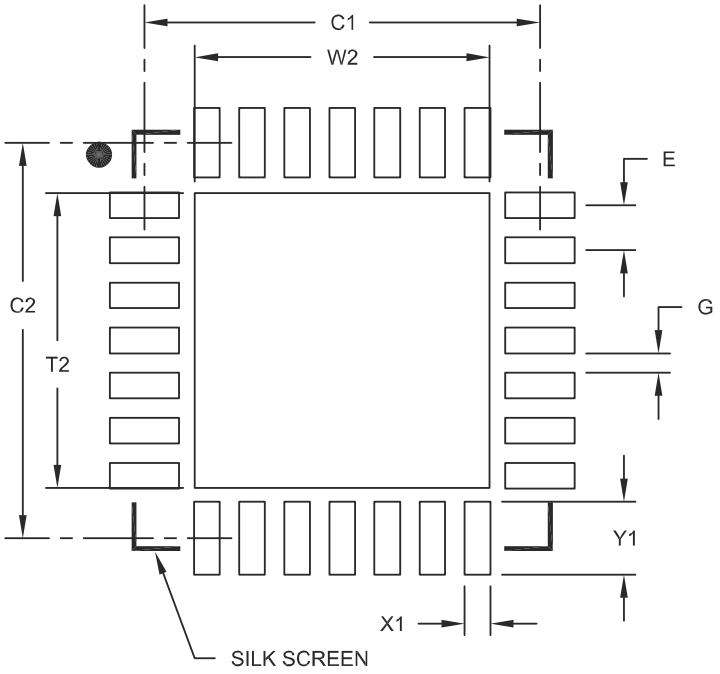
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

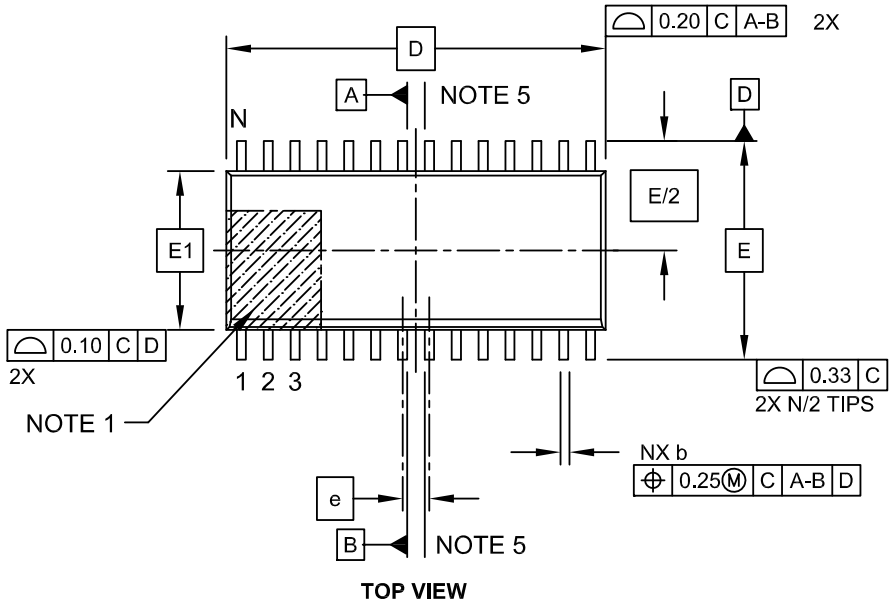
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

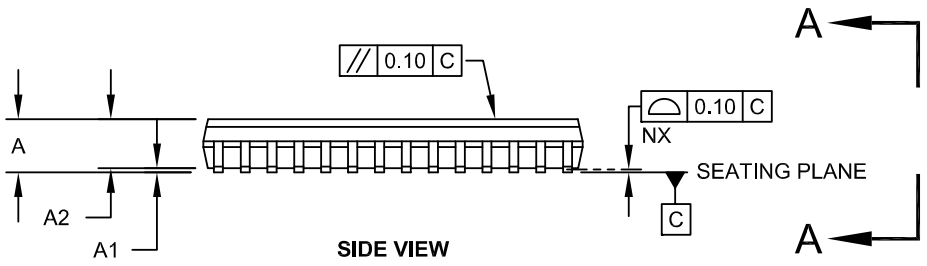
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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

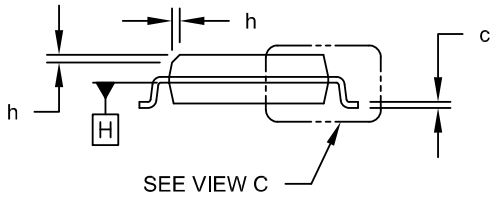
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



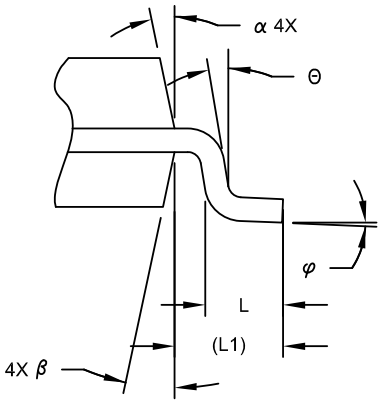
VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

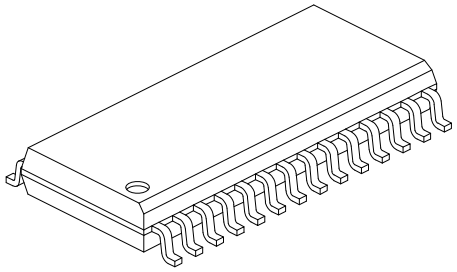
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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

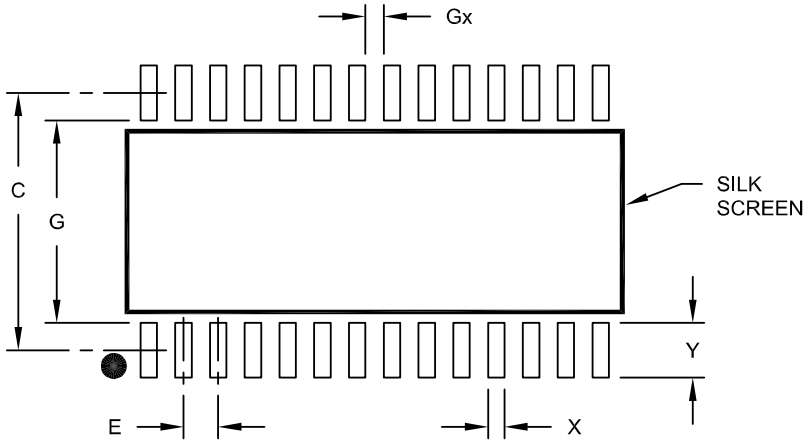
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

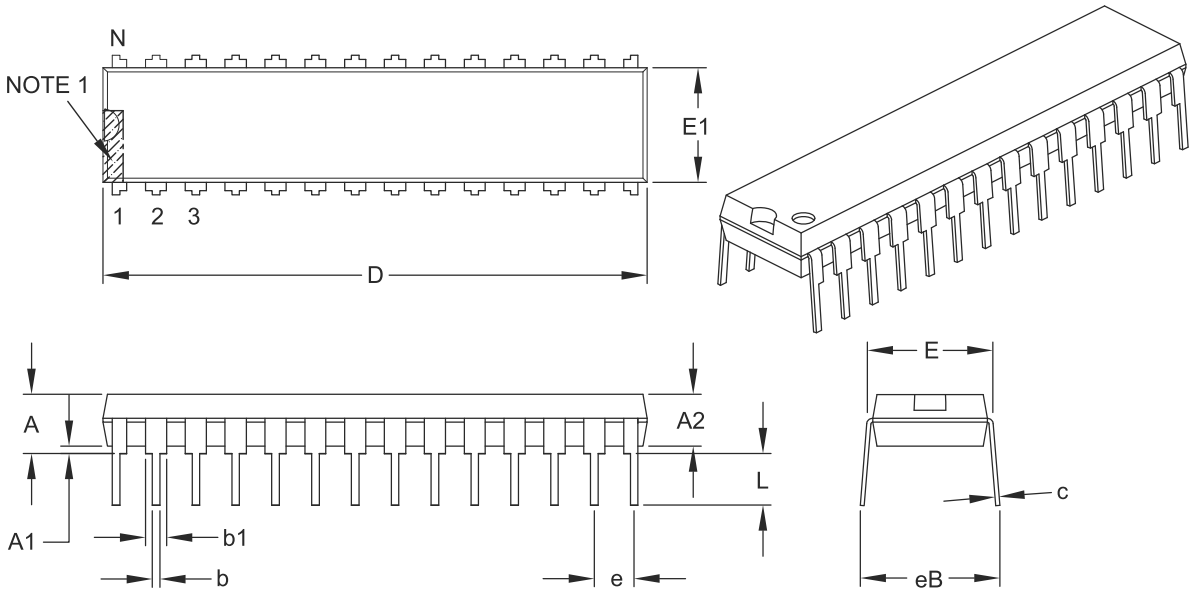
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

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28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

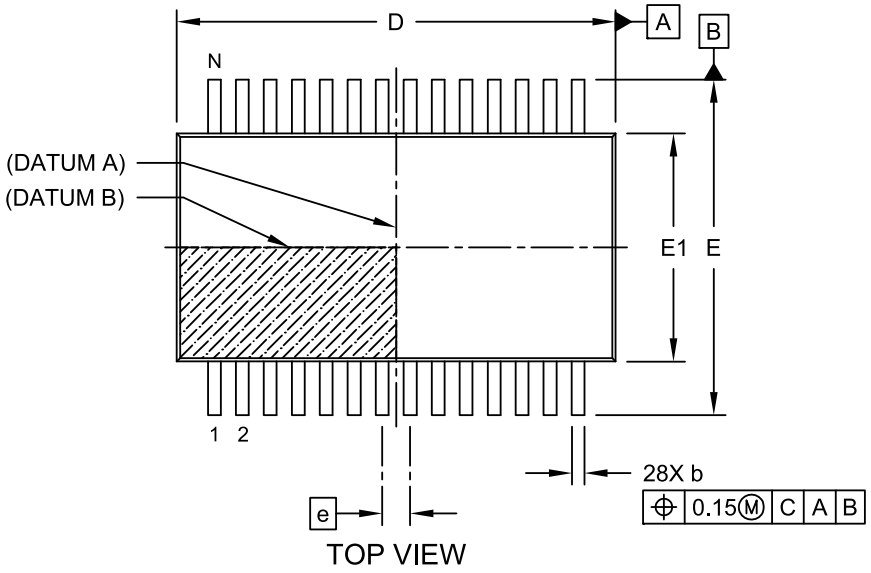
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

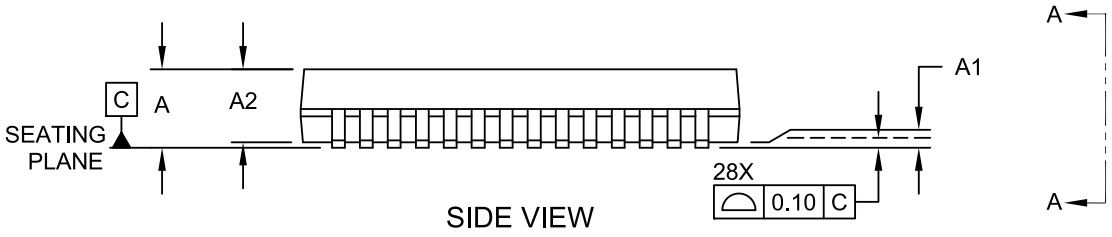
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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

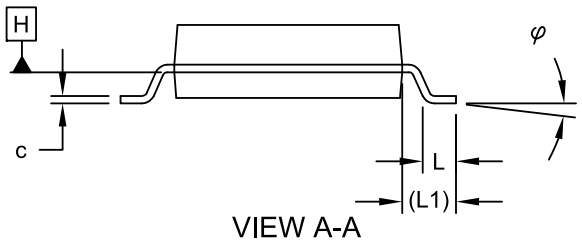
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



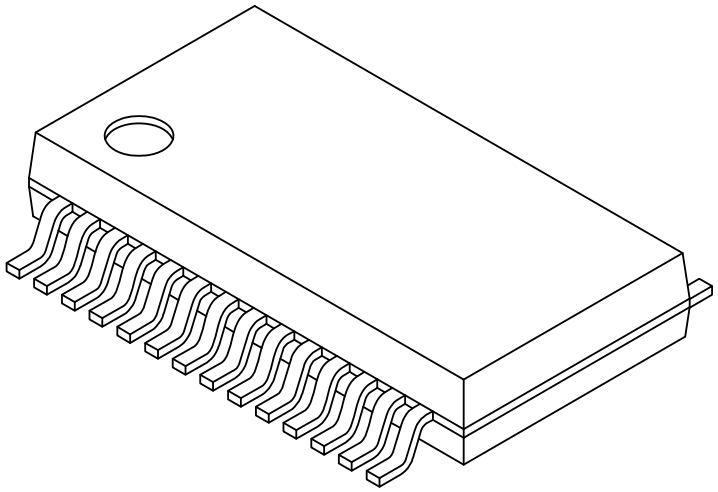
VIEW A-A

Microchip Technology Drawing C04-073 Rev C Sheet 1 of 2

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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

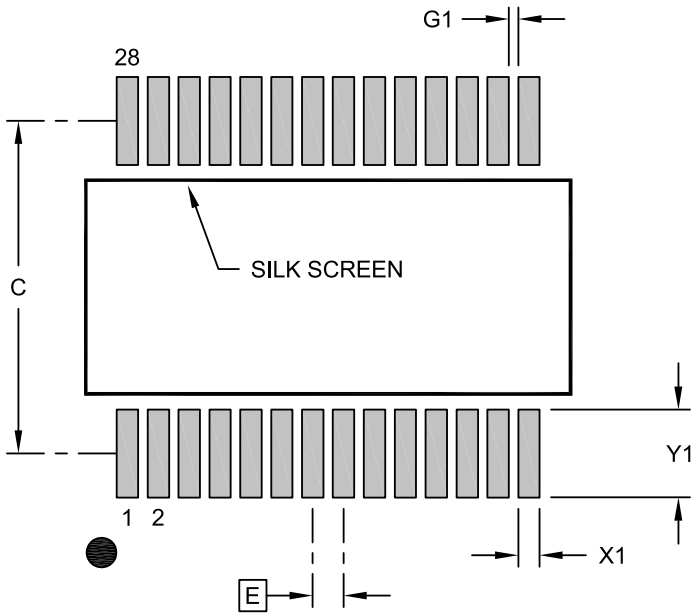
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073 Rev C Sheet 2 of 2

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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.00	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.85
Contact Pad to Center Pad (X26)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2073 Rev B

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APPENDIX A: REVISION HISTORY

Revision D (June 2022)

- Updated description in **Section "Features"**.
- Updated **Table 2-1**.
- Updated drawings for MCP23017 in **Section "Package Types"**.
- Updated **Section 3.5.1 "I/O Direction Register"**.
- Updated **Section 4.1 "Package Marking Information"**.
- Updated **Section "Product Identification System"**, with Automotive Qualified devices.
- Minor text and format changes throughout.

Revision C (July 2016)

- Added ESD data to **Section 1.0 "Electrical Characteristics"**.
- Updated **Table 2-1**.
- Updated package outline drawings.
- Minor typographical errors

Revision B (February 2007)

- Changed Byte and Sequential Read in **Figure 1-1** from "R" to "W".
- Table 2-4, Param No. 51 and 53: Changed from 450 to 600 and 500 to 600, respectively.
- Added disclaimers to package outline drawings.
- Updated package outline drawings.

Revision A (June 2005)

- Original release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] (1)	-X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Qualification

Device:	MCP23017:	16-Bit I/O Expander with I²C Interface	
	MCP23S17:	16-Bit I/O Expander with SPI Interface	
Tape and Reel Option:	T	=	Tape and Reel (1)
	Blank	=	Tube
Temperature Range:	E	=	–40°C to +125°C (Extended) *
	* While these devices are only offered in the "E" temperature range, the device will operate at different voltages and temperatures as identified in **Section 1.0 "Electrical Characteristics"**		
Package:	ML	=	Plastic Quad Flat, No Lead Package, 6x6 mm Body, QFN, 28-Lead
	SO	=	Plastic Small Outline, Wide, 7.50 mm Body, SOIC, 28-Lead
	SP	=	Skinny Plastic Dual In-Line, 300 mil Body, SPDIP, 28-Lead
	SS	=	Plastic Shrink Small Outline, 5.30 mm Body, SSOP, 28-Lead
Qualification:	<Blank>	=	Standard Part
	VAO	=	Automotive AEC-Q100 Qualified

Examples:

a)	MCP23017-E/ML:	Extended Temperature, 28-Lead QFN package
b)	MCP23017T-E/ML:	Tape and Reel, Extended temperature, 28-Lead QFN package
c)	MCP23017-E/SP:	Extended Temperature , 28-Lead SPDIP package
d)	MCP23017-E/SO:	Extended Temperature, 28-Lead SOIC package
e)	MCP23017T-E/SO:	Tape and Reel, Extended Temperature, 28-Lead SOIC package
f)	MCP23017-E/SS:	Extended Temperature, 28-Lead SSOP package
g)	MCP23017T-E/SS:	Tape and Reel, Extended Temperature, 28-Lead SSOP package
h)	MCP23017-E/SSVAO:	Extended Temperature, 28-Lead SSOP package, Automotive Qualified
i)	MCP23017T-E/SSVAO:	Tape and Reel, Extended Temperature, 28-Lead SSOP package, Automotive Qualified
j)	MCP23S17-E/ML:	Extended Temperature, 28-Lead QFN package
k)	MCP23S17T-E/ML:	Tape and Reel Extended Temperature, 28-Lead QFN package
l)	MCP23S17-E/SP:	Extended Temperature, 28-Lead SPDIP package
m)	MCP23S17-E/SO:	Extended Temperature, 28-Lead SOIC package
n)	MCP23S17T-E/SO:	Tape and Reel, Extended Temperature, 28-Lead SOIC package
o)	MCP23S17-E/SS:	Extended Temperature, 28-Lead SSOP package
p)	MCP23S17T-E/SS:	Tape and Reel, Extended Temperature, 28-Lead SSOP package
q)	MCP23S17-E/SSVAO:	Extended Temperature, 28-Lead SSOP package, Automotive Qualified
r)	MCP23S17T-E/SSVAO:	Tape and Reel, Extended Temperature, 28-Lead SSOP package, Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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Application Report
SLVA689–February 2015

I2C Bus Pullup Resistor Calculation

Rajan Arora

ABSTRACT

Pullup resistor calculation for I2C interface is a commonly asked question. In this application note we show how to use simple equations for this calculation.

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2 Pullup Resistor Calculation 2
3 Speed Versus Power Trade-off 4
4 Example 4

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1 Application Example Showing I2C Communication Between the Different IC's on a System and With Pullup Resistors on I2C Bus 2
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3 Maximum Pullup Resistance [R_P (max)] vs Bus Capacitance (C_b) 3

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Trademarks

1 Introduction

I2C communication standard is the mostly widely used inter-chip communication standard in today's electronic systems. It is an open-drain/open-collector communication standard which implies integrated circuits (IC's) with different voltage supply rails can be connected for communication. Pullup resistors need to be connected from the I2C lines to the supply to enable communication as shown in Figure 1. The pullup resistors pull the line high when it is not driven low by the open-drain interface. The value of the pullup resistor is an important design consideration for I2C systems as an incorrect value can lead to signal loss. In this article we show the simple equations for the pullup resistor calculation which the system designer can use to do quick calculations for their design.

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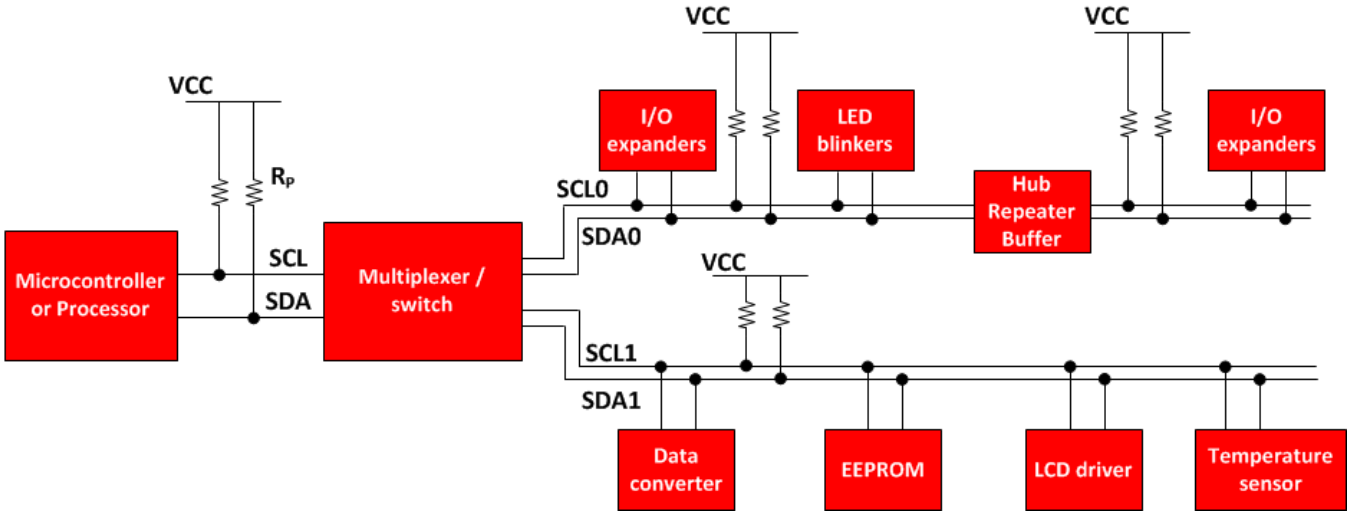


Figure 1. Application Example Showing I2C Communication Between the Different IC's on a System and With Pullup Resistors on I2C Bus

2 Pullup Resistor Calculation

A strong pullup (small resistor) prevents the I2C pin on an IC from being able to drive low. The V_{OL} level that can be read as a valid logical low by the input buffers of an IC determines the minimum pullup resistance [R_P(min)]. R_P(min) is a function of V_{CC}, V_{OL} (max), and I_{OL}:

$$R_P(\text{min}) = \frac{(V_{CC} - V_{OL}(\text{max}))}{I_{OL}} \quad (1)$$

The maximum pullup resistance is limited by the bus capacitance (C_b) due to I2C standard rise time specifications. If the pullup resistor value is too high, the I2C line may not rise to a logical high before it is pulled low. The response of an RC circuit to a voltage step of amplitude V_{CC}, starting at time t = 0 is characterized by time constant RC. The voltage waveform can be written as:

$$V(t) = V_{CC} \times \left(1 - e^{\frac{-t}{RC}}\right) \quad (2)$$

For $V_{IH} = 0.7 \times V_{CC}$:

$$V_{IH} = 0.7 \times V_{CC} = V_{CC} \times \left(1 - e^{\frac{-t1}{R_P \times C_b}}\right) \quad (3)$$

For $V_{IL} = 0.3 \times V_{CC}$:

$$V_{IL} = 0.3 \times V_{CC} = V_{CC} \times \left(1 - e^{\frac{-t2}{R_P \times C_b}}\right) \quad (4)$$

The rise time for the I2C bus can be written as:

$$t_r = t_2 - t_1 = 0.8473 \times R_p \times C_b \quad (5)$$

The maximum pullup resistance is a function of the maximum rise time (t_r):

$$R_p(\text{max}) = \frac{t_r}{(0.8473 \times C_b)} \quad (6)$$

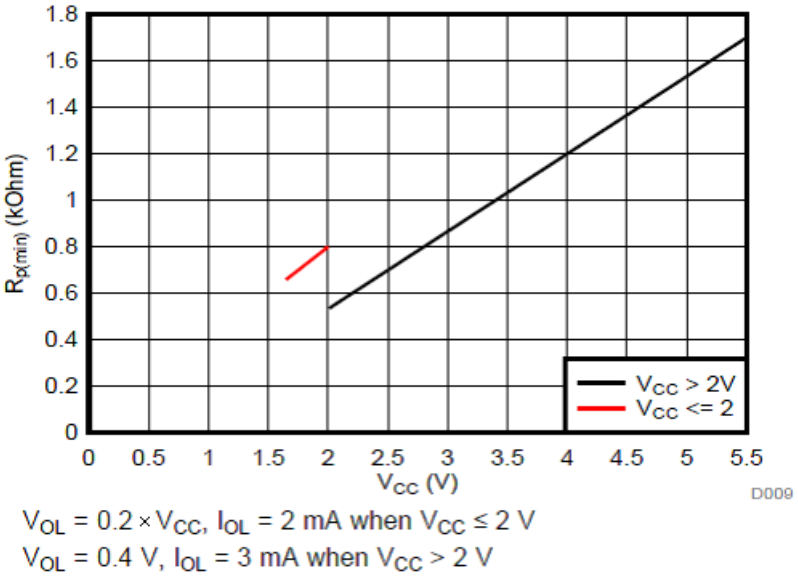
where parametrics from I2C specifications are listed in Table 1.

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Table 1. Parametrics from I2C specifications

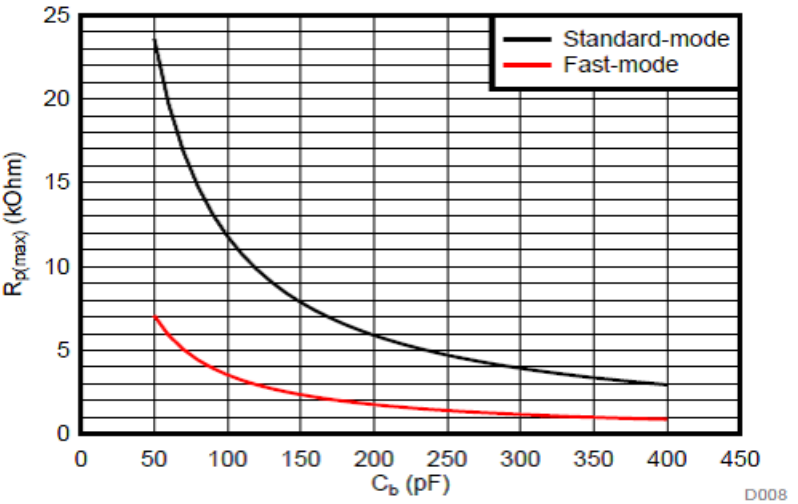
Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
t_r	Rise time of both SDA and SCL signals	1000	300	120	ns
C_b	Capacitive load for each bus line	400	400	550	pF
V_{OL}	Low-level output voltage (at 3 mA current sink, V_{CC} > 2 V)	0.4	0.4	0.4	V
	Low-level output voltage (at 2 mA current sink, V_{CC} ≤ 2 V)	–	0.2 × V_{CC}	0.2 × V_{CC}	V

The R_P (min) is plotted as a function of V_{CC} in Figure 2. The R_P (max) is plotted as a function of C_b in Figure 3 for standard-mode and fast-mode I2C.



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 2. Minimum Pullup Resistance [R_P (min)] vs Pullup Reference Voltage (V_{CC})



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)
Fast-mode (f_{SCL}= 400 kHz, t_r = 300 ns)

Figure 3. Maximum Pullup Resistance [R_P (max)] vs Bus Capacitance (C_b)

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3 Speed Versus Power Trade-off

Once the minimum and maximum value of the pullup resistor has been selected, the decision for the value of resistor can be made based on trade-off between the speed and power budget. A smaller resistor will give a higher speed because of smaller RC delay, and a larger resistor will give lower power consumption.

4 Example

For Fast-mode I2C communication with the following parameters, calculate the pullup resistor value.

C_b = 200 pF, V_{CC} = 3.3 V

Solution:

Taking the values from Table 1:

$$R_P(max) = \frac{t_r}{(0.8473 \times C_b)} = \frac{\left(300 \times 10^{-9}\right)}{\left(0.8473 \times 200 \times 10^{-12}\right)} = 1.77\ k\Omega \quad (7)$$

$$R_P(min) = \frac{V_{CC} - V_{OL}(max)}{I_{OL}} = \frac{(3.3 - 0.4)}{\left(3 \times 10^{-3}\right)} = 966.667\ \Omega \quad (8)$$

Therefore, we can select any available resistor value between 966.667 Ω and 1.77 kΩ. The value of the pullup resistor can be selected based on the trade-off for the power consumption and speed.

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Application Note

ESD and Surge Protection for USB Interfaces

Obi Oji *Multiplexers and Protection Devices*

ABSTRACT

Universal Serial Bus, more commonly known as USB, is an industry standard that defines communication, power supply, and connectors between computers and peripherals. There are many variations of USB standards that range from 1.5Mbps all the way up to 40Gbps with the more common standards being USB 2.0 and USB 3.x. There are also numerous connector types such as USB Type-A and USB Type-C®. With the recent European Union regulations, USB Type-C® is soon to be the single charging design for electronic devices in the EU, increasing the popularity of the connector. USB Type-C® is able to support alternate modes like DisplayPort, HMDI, and others as well as supporting USB Power Delivery (USB-PD) that allows for increased power transmission over USB.

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1 Overview

The Universal Serial Bus (USB) is an industry standard that specifies connection, communication, and power supply between host systems and peripherals. USB has evolved over the years through a series of standards focusing on increased data rates. The following table breaks down the standards including naming convention, data lines, nominal rates, and connector types.

There are two types of data pairs: half-duplex (HDx) and full-duplex (FDx). USB 2.0 and earlier standards use a single half-duplex which provides communication in both directions but only one direction at a time. A half-duplex translates to the D+ and D- data lines. USB 3.0 and later implement a single half-duplex (D+, D-) for USB 2.0 compatibility and two or four pairs in full-duplex with the full-duplex allowing for bidirectional communication simultaneously. A pair is considered to be either the transmit lines (TX+, TX-) or the receive lines (RX+, RX-). USB 3.0 and later include at least two pairs (TX+, TX-, RX+, RX-), also known as a lane.

Since there are many USB standards, determining the data rates can be confusing specifically for USB 3.2 and USB 4. The general consensus is that if the format is *AxB* then the last digit determines the number of lanes. For example, USB 3.2 Gen 2x2 has a nominal rate of 20Gbps, but since there is a *2* as the last digit, this means there are 2 data lanes each with 10Gbps totaling 20Gbps.

The following sections go into detail on ESD protection based on the nominal rate for USB interfaces.

Table 1-1. USB Standards

Standards	Data Pairs	Nominal Rate	USB-IF Name	Connector Types
USB 1.1	1 HDx	12Mbps	Basic-Speed USB	Type-A, Type-B
USB 2.0	1 HDx	480Mbps	Hi-Speed USB	Type-A, Type-B, Type-C, Micro, Mini
USB 3.0/USB 3.1 Gen 1/ USB 3.2 Gen 1x1	2 FDx + 1 HDx	5Gbps	USB 5Gbps	Type-A, Type-B, Type-C, Micro
USB 3.1 Gen 2/ USB 3.2 Gen 2x1	2 FDx + 1 HDx	10Gbps	USB 10Gbps	Type-A, Type-C
USB 3.2 Gen 1x2	4 FDx + 1 HDx	10Gbps	USB 10Gbps	Type-C
USB 3.2 Gen 2x2	4 FDx + 1 HDx	20Gbps	USB 20Gbps	Type-C
USB 4 Gen 2x1	2 FDx + 1 HDx	10Gbps	USB 10Gbps	Type-C
USB 4 Gen 2x2	4 FDx + 1 HDx	20Gbps	USB 20Gbps	Type-C
USB 4 Gen 3x1	2 FDx + 1 HDx	20Gbps	USB 20Gbps	Type-C

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2 USB 1.1

2.1 Overview

USB 1.0 was the first USB standard released with a revision, USB 1.1, shortly after. USB 1.0/1.1 has a 4-wire interface: V_{BUS} for power, D+ and D- for differential data signals, and a ground pin. USB 1.0/1.1 is able to support Low Speed (1.5Mbps) and Full Speed (12Mbps). Figure 2-1 details the pin configuration in a Type-A connector for USB 1.0/1.1.

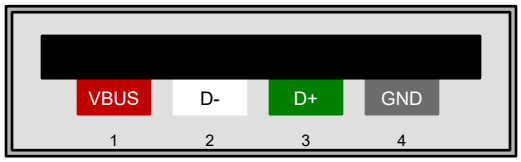


Figure 2-1. USB 1.0/1.1 Pin Configuration

USB 1.0/1.1 is a fairly uncommon standard used today in new systems but still at risk of high voltage strikes due to the external connector. An ESD strike can enter through the connector and can cause damage to the downstream components in the system. The following sections discuss the ESD protection requirements and the system-level design for USB 1.0/1.1.

2.2 ESD Protection Requirements

For protecting UBS 1.0/1.1, follow the list of parameters related to each pin:

- **D+ and D-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 1.0/1.1 data lines, the typical operating voltage is 3.3V. A working voltage greater than or equal to 3.3V is recommended.
  - Clamping Voltage: There can be many systems utilizing USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance: For USB 1.0/1/1, the signal speeds can reach up to 12Mbps. A capacitance less than 20pF is recommended to support the signal speed.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 1.0/1.1, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **V_{BUS}**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 2-1 lists devices that support these specifications.

Table 2-1. USB 1.0/1.1 Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523 (1.60 x 0.80)	D+, D-
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	VBUS
TPD4E05U06	5.5	12/15	0.5	4	USON (2.50 x 1.00)	D+, D-, VBUS

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2.3 System Level Design

TI offers ESD protection diodes with options to protect USB 1.0/1.1. Figure 2-2 shows a block diagram implementing three ESD protection diodes. The diodes are connected to each data and power line between the connector and either the battery charger or USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

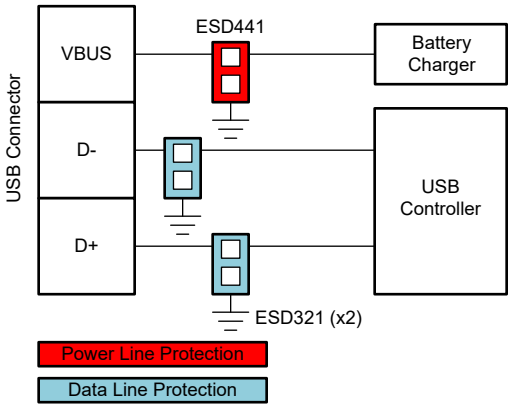


Figure 2-2. USB 1.0/1.1 ESD Protection

For Figure 2-2, ESD321 is used to the protect the D+ and D- lines and ESD441 is used to protect the VBUS line. There is also an option to use one ESD diode that protects both the data and power lines. For this to work, the diode is recommended to have a working voltage greater than or equal to 5V. A device that can handle both data and power lines is TPD4E05U06.

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3 USB 2.0 Circuit Protection

3.1 Overview

USB 2.0, also known as hi-speed USB, is an updated version of USB 1.0/1.1 with improved functionality and increased data speeds. USB 2.0 has a 4-wire interface: V_{BUS} for power, D+ and D- for differential data signals, and a ground pin. The pin configuration for USB 2.0 is shown in Figure 3-1 for a Type-A connector. USB 2.0 is able to support Low Speed (1.5Mbps), Full Speed (12Mbps), and High Speed (480Mbps).

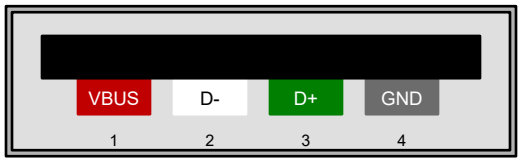


Figure 3-1. USB 2.0 Pin Configuration

USB 2.0 is a common interface still used today across a range of devices and applications. Since the connector is exposed to the outside world, the system is at risk of a high voltage strike. This transient event can cause damage to the downstream components in the system. The following sections discuss the ESD protection requirements and the system-level design for USB 2.0.

3.2 ESD Protection Requirements

For protecting UBS 2.0, follow the list of parameters related to each pin:

- **D+ and D-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 2.0 data lines, the typical operating voltage 3.3V. This translates to a working voltage of greater than or equal to 3.3V.
  - Clamping Voltage: There can be many systems utilizing USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance: Since the signal speeds for USB 2.0 can reach up to 480Mbps, a low-capacitance ESD diode with less than 4pF is recommended to support the signal speed.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 2.0, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **V_{BUS}**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 3-1 lists devices that support these specifications.

Table 3-1. USB 2.0 Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523(1.60 x 0.80)	D+, D-
ESD122	3.6	17/17	0.2	2	DFN1006, 3 pins (1.00 x 0.60)	D+, D-
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	VBUS
TPD4E05U06	5.5	12/15	0.5	4	USON (2.50 x 1.00)	D+, D-, VBUS

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3.3 System Level Designs

TI offers a multitude of ESD diodes with options to protect USB 2.0. Figure 3-2 shows a block diagram implementing three ESD protection diodes. The diodes are connected to each data and power line between the connector and either the battery charger or USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

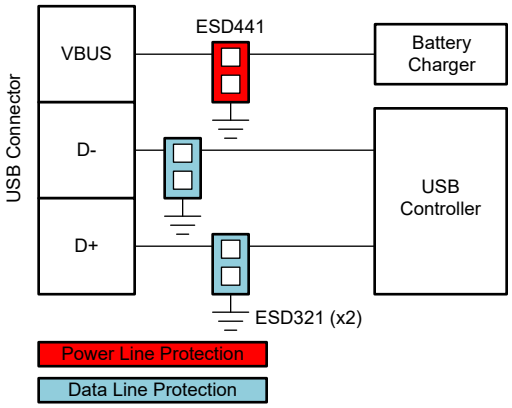


Figure 3-2. USB 2.0 ESD Protection

For the above diagram, ESD321 is used to the protect the D+ and D- lines and ESD441 is used to protect the VBUS line. There is also an option to use one ESD diode that protects both the data and power lines. For this to work, the diode is recommended to have a working voltage greater than or equal to 5V. A device that can handle both data and power lines is TPD4E05U06.

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4 USB 5Gbps

4.1 Overview

USB standards that reach a nominal rate of 5Gbps include: USB 3.0, USB 3.1 Gen 1, and USB 3.2 Gen 1x1. These standards use the following pins: V_{BUS} for power, D+ and D- for differential data signals, TX+, TX-, RX+, and RX- for transmitting and receiving signals, and ground.

USB 5Gbps is used in various devices and applications. There is an external connector which puts the system at risk of a high voltage strike. This transient event can cause damage to the downstream components in the system if the system is not protected properly. The following sections discuss the ESD protection requirements and the system-level design for protecting speeds up to 5Gbps.

4.2 ESD Protection Requirements

For protecting USB 5Gbps, follow the list of parameters related to each pin:

- **D+, D-, TX+, TX-, RX+, RX-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 5Gbps data lines, the typical operating voltage is 3.3V. A protection diode with a working voltage greater than or equal to 3.3V is recommended.
  - Clamping Voltage: There can be many systems utilizing USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance (D+, D-): Since D+ and D- are specific to USB 2.0 data transfer, the signal speeds can reach up to 480Mbps. An ESD diode with a capacitance less than 4pF is recommended.
  - Capacitance (TX+, TX-, RX+, RX-): The signal speeds can reach up to 5Gbps, a low-capacitance ESD diode with less than 0.5pF is recommended to support the signal speed.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 5Gbps, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **V_{BUS}**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 4-1 lists devices that support these specifications.

Table 4-1. USB 5Gbps Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523(1.60 x 0.80)	D+, D-
ESD122	3.6	17/17	0.2	2	DFN1006, 3 pins (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
TPD4E02B04	3.6	12/15	0.25	4	USON (2.50 x 1.00)	D+, D-, TX+, TX-, RX+, RX-
TPD6E05U06	5.5	12/15	0.47	6	USON (3.50 x 1.35)	D+, D-, TX+, TX-, RX+, RX-
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	VBUS

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4.3 System Level Designs

TI has a range of ESD diodes with options to protect USB 5Gbps. Figure 4-1 shows a block diagram implementing four ESD protection diodes. The diodes are connected to each data and power line between the connector and either the battery charger or USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

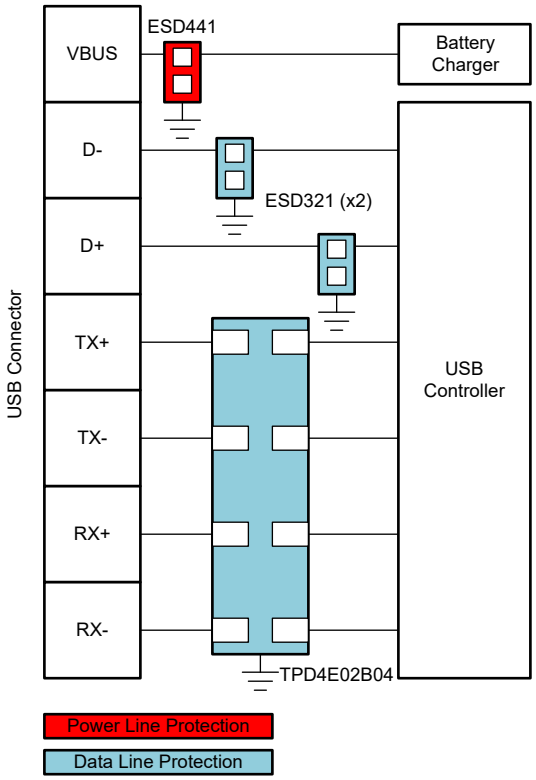


Figure 4-1. USB 5Gbps ESD Protection

For Figure 4-1, ESD321 is used to the protect D+ and D-. TPD4E02B04 is used for the TX/RX lines. There are a few other options for protecting the D/TX/RX lines such as using a 6-channel device, using multiple 2-channel devices, or even using 1-channel devices. ESD441 is used to protect the VBUS line.

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5 USB 10Gbps

5.1 Overview

USB standards that reach up to a nominal rate of 10Gbps are: USB 3.1 Gen 2, USB 3.2 Gen 2x1, USB 3.2 Gen 1x2, and USB 4 Gen 2x1. These standards use the following pins: V_{BUS} for power, D+ and D- for differential data signals, one lane (USB 3.1 Gen 2, USB 3.2 Gen 2x1, and USB 4 Gen 2x1) or two lanes (USB 3.2 Gen 1x2) for transmitting and receiving signals (TX1/RX1, TX2/RX2), and ground.

USB 10Gbps is commonly used today, and since there is an external connection, the system is at risk of a high voltage strike. An ESD strike can enter through the connector and cause damage to the downstream components if the system is not protected properly. The following sections discuss the ESD protection requirements and the system-level design for protecting USB 10Gbps signals.

5.2 ESD Protection Requirements

For protecting USB 10Gbps, follow the list of parameters related to each pin:

- **D+, D-, TX1+, TX1-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 10Gbps data lines, the typical operating voltage range is 3.3V. This translates to a working voltage of greater than or equal to 3.3V.
  - Clamping Voltage: There can be many systems utilizing USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance (D+, D-): Since D+ and D- are specific to USB 2.0 data transfer, the signal speeds can reach up to 480Mbps. An ESD diode with a capacitance less than 4pF is recommended.
  - Capacitance (TX+, TX-, RX+, RX-): Since the signal speeds can reach up to 10Gbps, a low-capacitance ESD diode with less than 0.3pF is recommended to support the signal speed. For USB 3.2 Gen 1x2, there are two lanes each with 5Gbps, a capacitance less than 0.5pF is recommended to support each lane.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 10Gbps, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **V_{BUS}**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 5-1 lists devices that support these specifications.

Table 5-1. USB 10Gbps Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523(1.60 x 0.80)	D+, D-
TPD1E01B04	3.6	15/17	0.18	1	DFN0603 (0.60 x 0.30), DFN1006 (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
ESD122	3.6	17/17	0.2	2	DFN1006, 3 pins (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
TPD4E02B04	3.6	12/15	0.25	4	USON (2.5 x 1.0)	D+, D-, TX+, TX-, RX+, RX-
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	VBUS

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5.3 System Level Designs

TI has a variety of ESD diodes that are able to protect USB 10Gbps. Figure 5-1 shows a block diagram implementing four ESD protection diodes. The diodes are connected to each data and power line between the connector and either the battery charger or USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

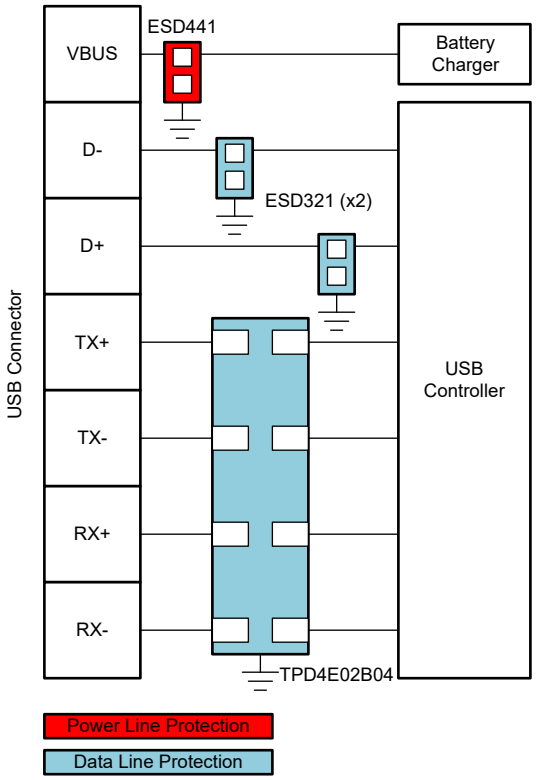


Figure 5-1. USB 10Gbps ESD Protection

For Figure 5-1, ESD321 is used to the protect D+ and D-. TPD4E02B04 is used for the TX/RX lines. There are a few other options for protecting the D/TX/RX lines such as using a 6-channel device, using multiple 2-channel devices, or even using 1-channel devices. ESD441 is used to protect the VBUS line.

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6 USB 20Gbps

6.1 Overview

USB standards that reach a nominal rate of 20Gbps are: USB 3.2 Gen 2x2, USB 4 Gen 2x2, and USB 4 Gen 3x1. These standards use the following pins: V_{BUS} for power, D+ and D- for differential data signals, one lane (USB 4 Gen 3x1) or two lanes (USB 3.2 Gen 2x2 and USB 4 Gen 2x2) for transmitting and receiving signals (TX1/RX1, TX2/RX2), and ground.

USB 20Gbps is used in a range of devices and applications. Since there is a connection exposed to the outside world, there is a risk of a high voltage strike occurring. An transient event can cause damage to the downstream components in the system. The following sections discuss the ESD protection requirements and the system-level design for protecting speeds up to 20Gbps.

6.2 ESD Protection Requirements

For protecting USB 20Gbps, follow the list of parameters related to each pin:

- **D+, D-, TX1+, TX1-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For USB 20Gbps data lines, the typical operating voltage is 3.3V. This translates to a working voltage of greater than or equal to 3.3V.
  - Clamping Voltage: There can be many systems utilizing USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance (D+, D-): Since D+ and D- are specific to USB 2.0 data transfer, the signal speeds can reach up to 480Mbps. An ESD diode with a capacitance less than 4pF is recommended.
  - Capacitance (TX+, TX-, RX+, RX-): For USB 4 Gen 3x1, the signal speeds can reach up to 20Gbps meaning an ultra low capacitance ESD diode with less than 0.25pF is recommended. For the two lane standards that reach up to 10Gbps per lane, a very low capacitance ESD diode with less than 0.3-pF is recommended.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. For USB 20Gbps, a minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **V_{BUS}**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 6-1 lists devices that support these specifications.

Table 6-1. USB 20Gbps Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523(1.60 x 0.80)	D+, D-
TPD1E01B04	3.6	15/17	0.18	1	DFN0603 (0.60 x 0.30), DFN1006 (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
ESD122	3.6	17/17	0.2	2	DFN1006, 3 pins (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
TPD4E02B04	3.6	12/15	0.25	4	USON (2.5 x 1.0)	D+, D-, TX/RX for 10-Gbps per lane
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	VBUS

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6.3 System Level Designs

TI has an array of ESD diodes able to protect USB 20Gbps. Figure 6-1 shows a block diagram implementing multiple ESD protection diodes. The diodes are connected to each data and power line between the connector and either the battery charger or USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

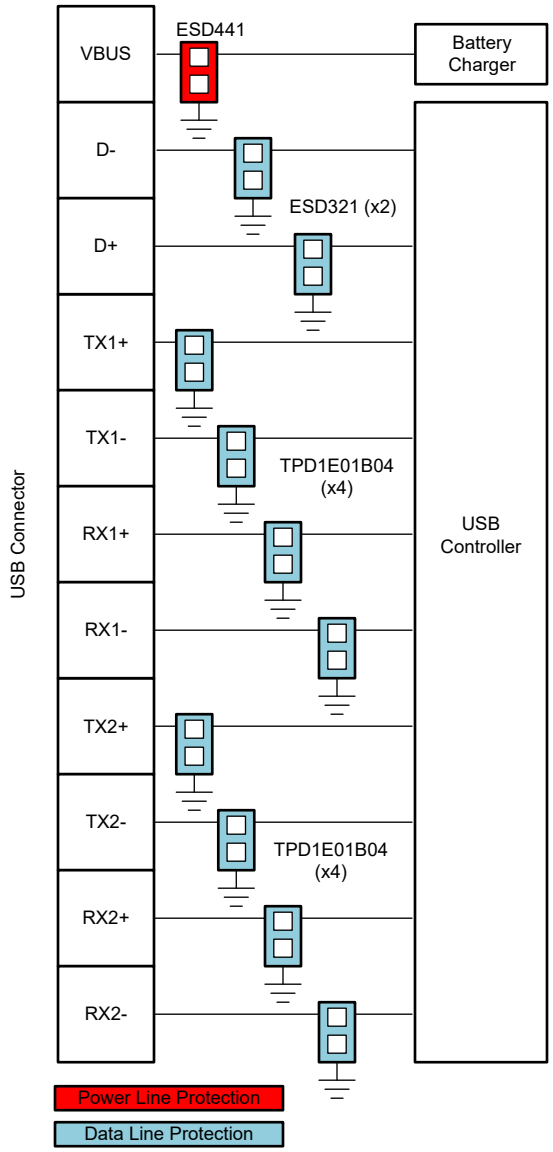


Figure 6-1. USB 20Gbps ESD Protection

For Figure 6-1, ESD321 is used to the protect the D+ and D- lines, eight TPD1E01B04's are used to protect the TX/RX lines, and ESD441 is used to protect the VBUS line. The possibilities are endless for protecting the USB lines and can use multi-channel or single-channel protection diodes.

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7 USB Type-C® Protection

7.1 Overview

USB Type-C® is a 24-pin connector that allows for transmission of large amounts of power and data on a single cable. USB Type-C® is able to support USB 2.0 and all standards after as well as alternate modes like HDMI and DisplayPort. The standard also supports the USB-PD standard which is primarily implemented on the USB Type-C connector. Figure 7-1 details the pin configuration for the USB Type-C® connector.

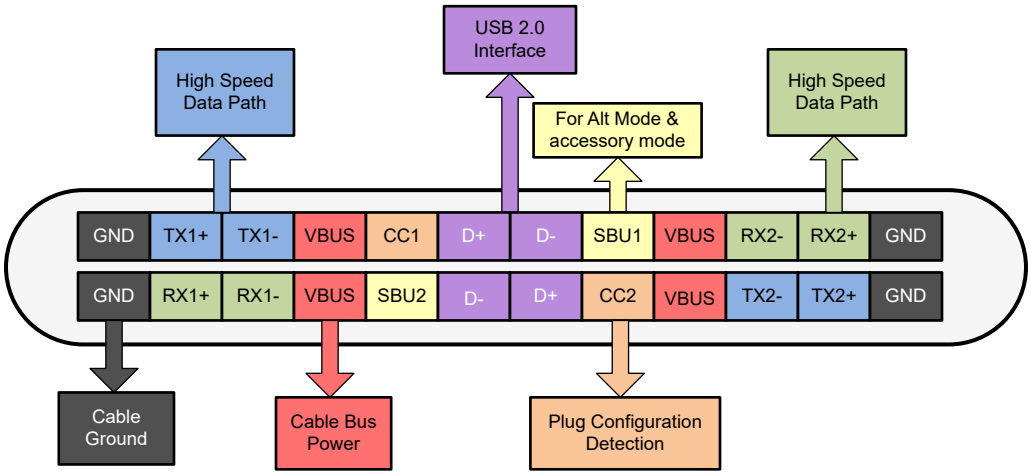


Figure 7-1. USB Type-C® Pin Configuration

While USB Type-C® incorporates the same pins mentioned throughout the application note such as D+ and D- and the TX/RX lines, there are additional pins specific to USB Type-C®: CC1/CC2 and SBU1/SBU2. The CC pins are the channel configuration pins. The pins are able to detect cable attachment, cable orientation, and current advertisement. The SBU pins are for sideband use. The pins are used in audio adapter accessory mode and alternate modes. The alternate modes include DisplayPort, HDMI, and Thunderbolt. The following section means the ESD protection requirements to properly protect a USB Type-C® connector.

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7.2 ESD Protection Requirements

For protecting USB Type-C®, follow the list of parameters related to each pin:

- **D+, D-, TX1+, TX1-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. For data lines, the typical operating voltage range is 3.3V. This translates to a working voltage of greater than or equal to 3.3V.
  - Clamping Voltage: There can be many systems using USB. This results in the clamping voltage of the ESD diode being dependent on the circuity downstream from the USB connector. The clamping voltage is recommended to be below the absolute maximum rating of the downstream component.
  - Capacitance (D+, D-): Since D+ and D- are specific to USB 2.0 data transfer, the signal speeds can reach up to 480Mbps. An ESD diode with a capacitance less than 4pF is recommended.
  - Capacitance (TX+, TX-, RX+, RX-): For speeds up to 5Gbps per lane, the capacitance is recommended to be less than 0.5pF. For 10Gbps per lane, the capacitance is recommended to be less than 0.3pF, and 20Gbps per lane, the capacitance is recommended to be less than 0.25pF.
  - IEC 61000-4-2 Rating: Real-world ESD strikes are defined by the IEC 61000-4-2 testing standard. This standard consists of two measurements: contact and air-gap discharge. The higher the contact and air-gap rating, the higher the voltage a device can withstand. A minimum IEC 61000-4-2 rating of 8kV for contact and 15kV for air-gap is recommended.
- **CC**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. The typical operating voltage for the CC pins can reach up to 5V. This translates to a working voltage of greater than or equal to 5V.
- **SBU**
  - Working Voltage: The reverse working voltage (V_{RWM}) of the protection diode is recommended to be greater than or equal to the operating voltage of the system being protected. The typical operating voltage for the SBU pins is up to 3.6V. This translates to a working voltage of greater than or equal to 3.6V.
  - Capacitance: Due to higher data speeds on the SBU lines, a low capacitance diode is needed. Depending on the signal speed, the capacitance can vary. For speeds up to 5Gbps, a capacitance less than 0.5pF is recommended.
- **VBUS**
  - Working Voltage: For V_{BUS}, the operating voltage is 5V. An ESD diode with a working voltage greater than or equal to 5V is recommended.

Table 7-1. USB Type-C® Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD321	3.6	30/30	0.9	1	DFN1006 (1.00 x 0.60), SOD523(1.60 x 0.80)	D+, D-
TPD1E01B04	3.6	15/17	0.18	1	DFN0603 (0.60 x 0.30), DFN1006 (1.00 x 0.60)	D+, D-, TX+, TX-, RX+, RX-
TPD4E02B04	3.6	12/15	0.25	4	USON (2.5 x 1.0)	D+, D-, TX+, TX-, RX+, RX-
ESD341	3.6	30/30	0.66	1	DFN0603 (0.60 x 0.30)	SBU
ESD441	5.5	30/30	1	1	DFN0603 (0.60 x 0.30)	CC, VBUS

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7.3 System Level Designs

TI has a variety of ESD protection diodes able to protect each pin of a USB Type-C® connector. Figure 7-2 shows a block diagram implementing single-channel ESD protection diodes. The diodes are connected to each data and power line between the connector and USB controller. To properly protect the system, place the diodes as close to the source of ESD, in this case the connector, as design rules allow.

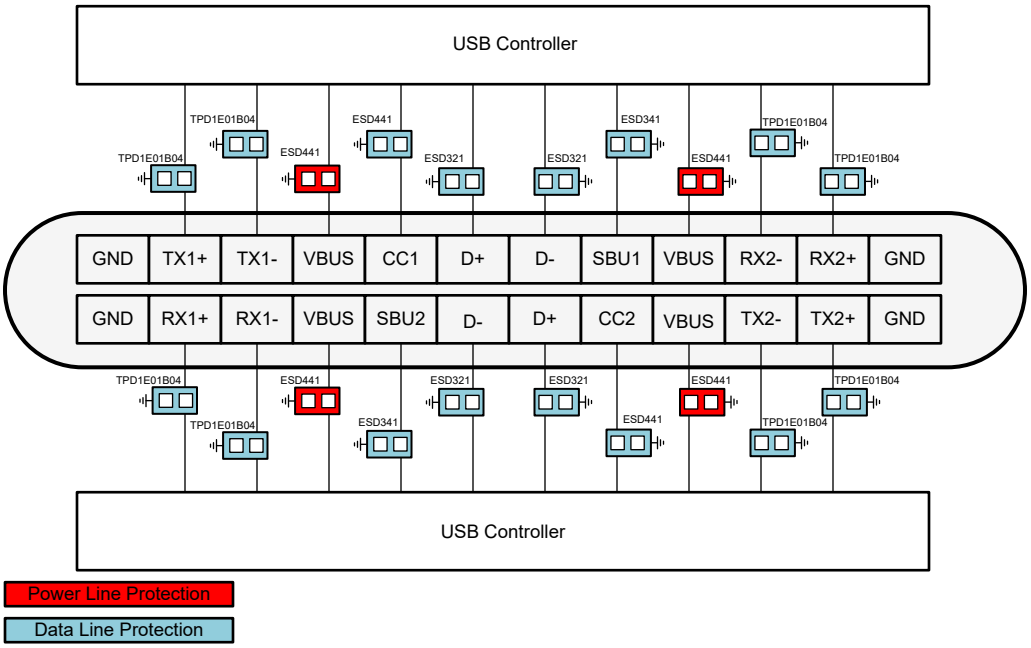


Figure 7-2. USB Type-C® ESD Protection

For Figure 7-2, TPD1E04B04 is used to protect the TX/RX lines, ESD321 is used for the D+ and D- lines, ESD441 is protecting the CC pins and VBUS, and ESD341 is used to protect the SBU pins. There are many options for protecting USB Type-C® including using multi-channel devices.

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8 USB Power Delivery (USB-PD) Surge Protection

8.1 Overview

Over the years, the USB standard has become an interface that not only allows data to be transferred but one that allows for transfer of power. In USB 2.0 and USB 3.x standards, the maximum power that can be delivered is 15W, with a maximum of 5V on V_{BUS}. The USB-Power Delivery (USB-PD) standard allows for more power (up to 240 W) to be supplied to systems over a compliant USB cable. The voltage on the V_{BUS} pin can vary depending on the power that needs to be supplied. Common voltages are 5V, 9V, 15V, and 20V and more recently 28V, 36V, and 48V.

8.2 VBUS Protection

As with all power lines, consideration must be taken about how to protect against transient over voltage events. For example, when there is a plug or unplug event while there is current flowing through the cable, inductive ringing can cause a 20V line to temporarily go up to 50V which can damage downstream circuitry. A recommendation to protect the system is to use a protection diode and a key specification to consider is the clamping voltage, confirming the voltage experienced by the system is below the maximum voltage of the system. The TVS2200 is a device that protects a 20V line with a very low clamping voltage. This results in the system seeing a maximum voltage of 28V during a transient event. The plots in Figure 8-1 and Figure 8-2 show the result and benefits of using a TVS device. Also, Table 8-1 shows recommended TVS diodes for USB-PD voltage levels.

Table 8-1. USB-PD VBUS Surge Protection Recommendations

USB-PD Voltage	Recommended TVS	Surge Clamping Voltage	Package | Size
5V	TVS0500	9V	DRV | 2 × 2 mm
9V	TVS1400	18V	DRV |2 × 2 mm
15V	TVS1800	23V	DRV | 2 × 2 mm
20V	TVS2200	28V	DRV | 2 × 2 mm
28V	TVS3300	38V	DRV | 2 × 2 mm YZF | 1.1 × 1.1 mm

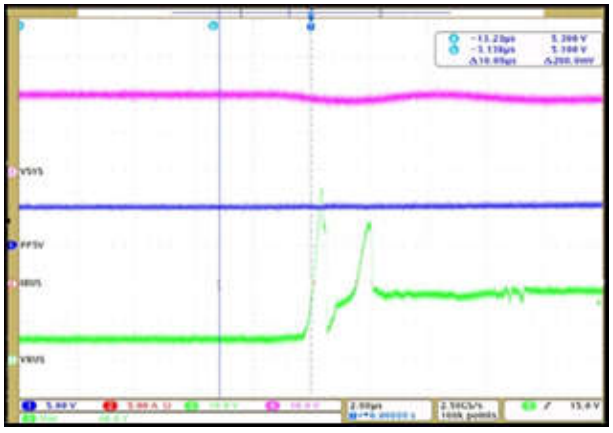


Figure 8-1. USB-PD VBUS Over Voltage Event Without TVS

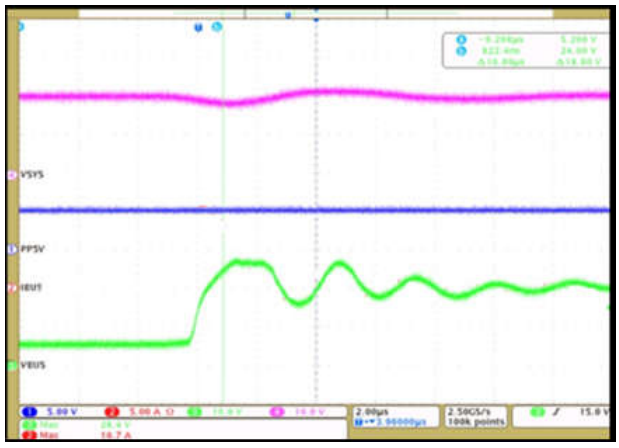


Figure 8-2. USB-PD VBUS Over Voltage Clamped by TVS2200

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8.3 Short to VBUS

Protecting against a short to V_{BUS} is another care about. In the case of short to V_{BUS}, the CC and SBU pins can be exposed to the voltage on V_{BUS} due to the proximity to V_{BUS}. Figure 8-3 represents a cause of a short to VBUS event such as removing the connector improperly.

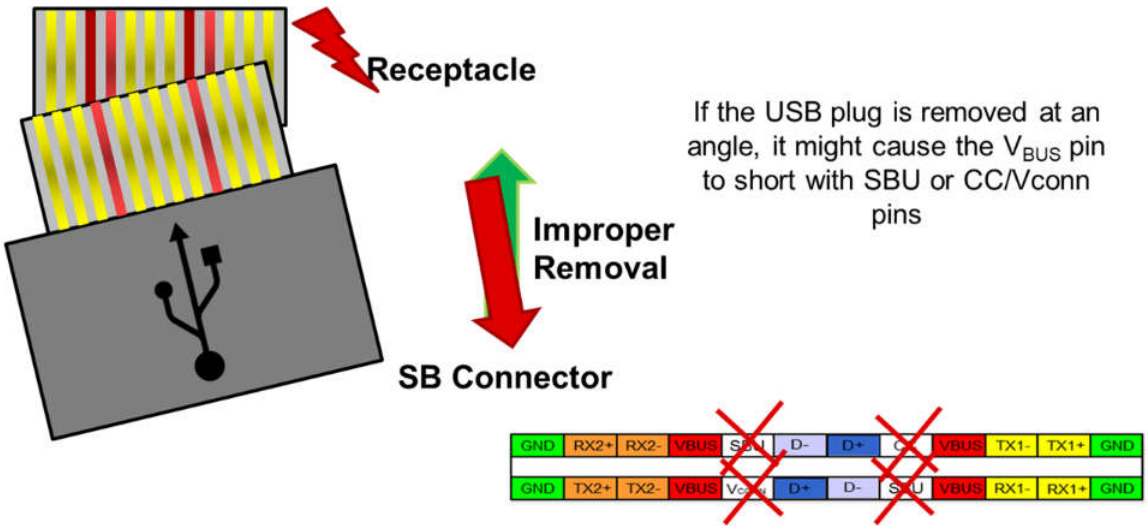


Figure 8-3. Short to VBUS

As mentioned, the voltages for USB-PD can be in the range of 5V all the way up to 48V. This requires the same working voltage of a protection diode across CC, SBU, and VBUS pins to verify the system is protected from ESD. Device recommendations for these conditions are shown in Table 8-2. For more devices on short to V_{BUS} protection, check out the USB-PD team at TI.

Table 8-2. Short to VBUS Device Recommendations

Device	V_{RWM} (V)	IEC 61000-4-2 (kV) (Contact/Air-gap)	Capacitance (pF)	Channel Count	Package Size (mm)	Recommended For
ESD2CAN24-Q1 / ESD752	24	30/30	3	2	SOT023 (2.92 x 2.37), SOT-SC70 (2.0 x 2.1)	VBUS, CC, SBU

9 References

- Texas Instruments, *A primer on USB Type-C® and USB Power Delivery Applications and Requirements*, marketing white paper.
- Texas Instruments, *System-Level ESD Protection Guide*.
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*, user's guide.
- Texas Instruments, *ESD Packaging and Layout Guide*, application note.

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10 Revision History

Changes from Revision A (August 2022) to Revision B (January 2024)	Page
• Added and updated information on USB to include the majority of protocols as well as added device recommendations for each protocol	1

Changes from Revision * (November 2021) to Revision A (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *ESD341* to the *USB 2.0 Data Line Protection Recommendations* table	6

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